MOBILE INTEL® CELERON® PROCESSOR IN MICRO-PGA AND BGA PACKAGES AT 466 MHZ, 433 MHZ, 400 MHZ, 366 MHZ, 300 MHZ, AND 266 MHZ DATASHEET

- **Available at 266 MHz, 266 MHz at low voltage, 300 MHz, 333 MHz, 366 MHz, 400 MHz, 433 MHz, and 466 MHz**
- **Supports Intel Architecture with Dynamic Execution**
- **Integrated primary 16-Kbyte instruction cache and 16-Kbyte write back data cache**
- **Integrated second level cache (128-Kbyte)**
- **Micro-PGA and BGA packaging technology**
  - **Supports thin form factor notebook designs**
  - **Exposed die enables more efficient heat dissipation**
- **Fully compatible with previous Intel microprocessors**
  - **Binary compatible with all applications**
  - **Support for MMX™ technology**
- **Power Management Features**
  - **Quick Start and Deep Sleep modes provide extremely low power dissipation**
- **Low-Power GTL+ processor system bus interface**
- **Integrated math co-processor**
- **Integrated thermal diode**

The mobile Intel® Celeron® (Micro-PGA and BGA) processor provides exceptional value to both businesses and consumers. The mobile Intel Celeron processor with multimedia enhancements and improved Internet and communications capabilities not only provides an excellent solution for business but also a great choice for home computing.

The mobile Intel Celeron (Micro-PGA and BGA) processor may contain design defects or errors know as errata that may cause the product to deviate from published specifications. Current characterized errata are available upon request.

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1. INTRODUCTION

The mobile Intel Celeron processor is the first mobile processor with an integrated L2 cache among the mobile processors. The mobile Intel Celeron processor is now offered at seven speeds: 466 MHz, 433 MHz, 400 MHz, 366 MHz, 333 MHz, 300 MHz, and 266 MHz, with a system bus speed of 66 MHz. It consists of a mobile Intel Celeron processor with an integrated L2 cache and a 64-bit high performance system bus. The integrated L2 cache is designed to help improve performance, it complements the system bus by providing critical data faster and reducing total system power consumption. The mobile Intel Celeron processor's 64-bit wide Low Power Gunning Transceiver Logic (GTL+) system bus is compatible with the 443BX/DX/440MX AGPSet and provides a glue-less, point-to-point interface for an I/O bridge/memory controller. Figure 1.1 shows the various parts of a mobile Intel Celeron processor-based system and how the mobile Intel Celeron processor connects to them.

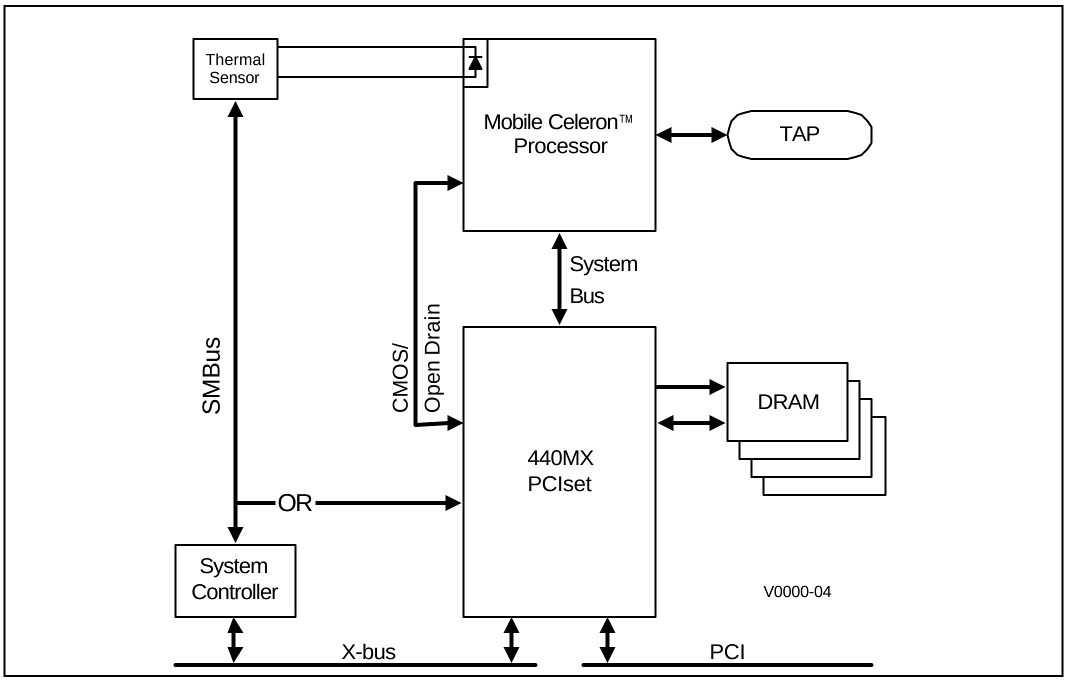


Figure 1.1 Signal Groups of a Mobile Intel Celeron Processor-Based System

1.1 Overview

- Exceptional value and improved performance over existing mobile processors
  - Supports the Intel Architecture with Dynamic Execution
  - Supports the Intel Architecture MMX™ technology
  - Integrated Intel Floating-Point Unit compatible with the IEEE Std 754
- Integrated primary (L1) instruction and data caches
  - 4-way set associative, 32-byte line size, 1 line per sector
  - 16-Kbyte instruction cache and 16-Kbyte writeback data cache
  - Cacheable range programmable by processor programmable registers
- Integrated second level (L2) cache
  - 4-way set associative, 32-byte line size, 1 line per sector
  - Operates at full core speed
  - 128-Kbyte, ECC protected cache data array
  - 4-Gbyte cacheable range
- Low Power GTL+ system bus interface
  - 64-bit data bus, 66-MHz operation
  - Uniprocessor, two loads only (processor and I/O bridge/memory controller)
  - Short trace length and low capacitance allows for single ended termination
- Voltage reduction technology
- Advanced processor clock control
  - Quick Start for low power, low exit latency clock “throttling”
  - Deep Sleep mode for extremely low power dissipation
- Thermal diode for measuring processor temperature

1.2 Terminology

In this document a ‘#’ symbol following a signal name indicates that the signal is active low. This means that when the signal is asserted (based on the name of the signal) it is in an electrical low state. Otherwise, signals are driven in an electrical high state when they are asserted. In state machine diagrams, a signal name in a condition indicates the condition of that signal being asserted. If the signal name is preceded by a ‘!’ symbol, then it indicates the condition of that signal not being asserted. For example, the condition ‘!STPCLK# and HS’ is equivalent to ‘the active low signal STPCLK# is unasserted (i.e., it is at 2.5V) and the HS condition is true.” The symbols ‘L’ and ‘H’ refer respectively to electrical low and electrical high signal levels. The symbols ‘0’ and ‘1’ refer respectively to logical low and logical high signal levels. For example, BD[3:0] = ‘1010’ = ‘HLHL’ refers to a hexadecimal ‘A’, and D[3:0]# = ‘1010’ = ‘LHLH’ also refers to a hexadecimal ‘A’.

1.3 References

Pentium® II Processor at 233 MHz, 266 MHz, 300 MHz and 333 MHz (Order Number 243335)

Pentium® II Processor Developer’s Manual (Order Number 243502)

CKDM66-M Clock Driver Specification (Contact your Intel Field Sales Representative)

Intel Architecture Software Developer’s Manual (Order Number 243193)

Volume I: Basic Architecture (Order Number 243190)
Volume II: Instruction Set Reference (Order Number 243191)
Volume III: System Programming Guide (Order Number 243192)

Mobile Intel® Celeron® Processor I/O Buffer Models, IBIS Format (Available in electronic format; contact your Intel Field Sales Representative)

Mobile Pentium® II Processor System Bus Layout Guideline (Order Number 243672-001)

Mobile Pentium® II Processor Mechanical and Thermal User's Guide (Order Number 243671-001)

2. MOBILE INTEL CELERON PROCESSOR FEATURES

2.1 New Features in the Mobile Intel Celeron Processor

New features include an integrated L2 cache and various signal differences from the mini-cartridge processors.

2.1.1 Integrated L2 Cache

The mobile Intel Celeron processor has a 128-Kbyte L2 cache integrated onto the processor die. The L2 cache is four-way set associative and runs at the speed of the processor core. The L2 cache can cache up to 4 Gbytes of memory.

2.1.2 Signal Differences from the Mini-Cartridge Processors

Table 2.1 New Mobile Intel Celeron Processor Signals

Signals	Purpose
EDGCTRLN	GTL+ output buffer edge rate control signals
NC	No Connect (same as RSVD signals on mini-cartridge)
BSEL	Bus speed select
TESTHI, TESTHI3	Testability signals. Pull-up to V_{CC}.
TESTHI2	Testability signals. Pull-up to V_{CCP}.
TESTLO	Testability signals. Connect to V_{SS}.
THERMDA, THERMDC	Thermal diode
PLL1, PLL2	PLL analog power supply
V_{REF}	GTL+ reference voltage

Table 2.2 Removed Mini-Cartridge Processor Signals

Signals	Purpose
SMBALERT#, SMBCLK, SMBDATA	SMBus interface for the thermal sensor
V_{CC_S}, V_{CCP_S}, V_{SS_S}	Voltage sense signals
V_{CC3}	3.3V supply for external L2 cache components
VID[3:0]	Voltage identification

2.2 Power Management

2.2.1 Clock Control Architecture

The mobile Intel Celeron processor clock control architecture (Figure 2.1) has been optimized for leading edge deep green desktop and mobile computer designs. The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep, and Deep Sleep states. The Auto Halt state provides a low-power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low power, low exit latency clock state that can be used for hardware controlled "idle" computer states. The Deep Sleep state provides an extremely low-power state that can be used for "Power-On Suspend" computer states, which is an alternative to shutting off the processor's power. Compared to the Pentium processor exit latency of 1 msec, the exit latency of the Deep Sleep state has been reduced to 30 µsec in the mobile Intel Celeron processor. The Stop Grant and Sleep states shown are intended for use in "Deep Green" desktop and server systems — not in mobile systems. Performing state transitions not shown in Figure 2.1 is neither recommended nor supported.

The Stop Grant and Quick Start clock states are mutually exclusive, for example a strapping option on signal A15# chooses which state is entered when the STPCLK# signal is asserted. Strapping the A15# signal to ground at Reset enables the Quick Start state; otherwise, asserting the STPCLK# signal puts the processor into the Stop Grant state. The Stop Grant state has a higher power level than the Quick Start state and is designed for SMP platforms. The Quick Start state has a much lower power level, but it can only be used in uniprocessor platforms.

2.2.2 Normal State

The Normal state of the processor is the normal operating mode where the processor's internal clock is running and the processor is actively executing instructions.

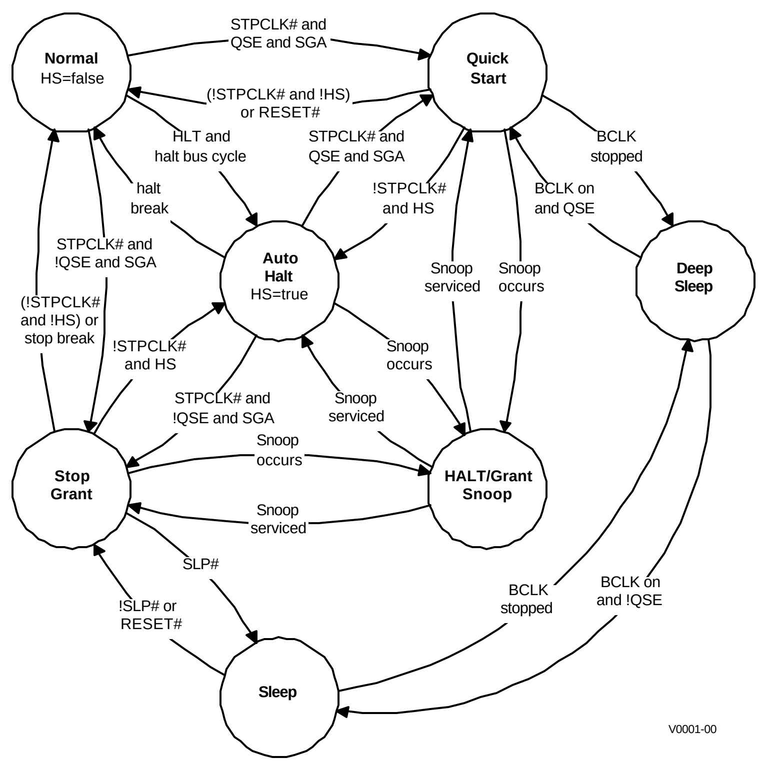
2.2.3 Auto Halt State

This is a low-power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Stop Grant or Quick Start state, where a Stop Grant Acknowledge bus cycle will be issued. Deasserting STPCLK# will cause the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# interrupt is recognized in the Auto Halt state. The return from the System Management Interrupt (SMI) handler can be to either the Normal state or the Auto Halt state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from System Management Mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After the on-chip and off-chip caches have been flushed, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.



NOTES: Halt break - A20M#, BINIT#, FLUSH#, INIT#, INTR, NMI, PREQ#, RESET#, SMI#
HLT - HLT instruction executed
HS - Processor Halt State
QSE - Quick Start State Enabled
SGA - Stop Grant Acknowledge bus cycle issued
Stop break - BINIT#, RESET#

Figure 2.1 Clock Control States

Table 2.3 Clock State Characteristics

Clock State	Exit Latency	Snooping?	System Uses
Normal	N/A	Yes	Normal program execution
Auto Halt	Approximately 10 bus clocks	Yes	S/W controlled entry idle mode
Stop Grant	Approximately 10 bus clocks	Yes	H/W controlled entry/exit mobile throttling
Quick Start	Through snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 8 bus clocks	Yes	H/W controlled entry/exit mobile throttling
HALT/Grant Snoop	A few bus clocks after the end of snoop activity.	Yes	Supports snooping in the low power states
Sleep	To Stop Grant state, 10 bus clocks	No	H/W controlled entry/exit desktop idle mode support
Deep Sleep	30 µsec	No	H/W controlled entry/exit mobile powered-on suspend support

2.2.4 Stop Grant State

The processor enters this mode with the assertion of the STPCLK# signal when it is configured for Stop Grant state (via the A15# strapping option). The processor is still able to respond to snoop requests and it can latch interrupts. Latched interrupts will be serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event will be latched. A transition back to the Normal state can be made by the deassertion of the STPCLK# signal or the occurrence of a stop break event (a BINIT# or RESET# assertion).

The processor will return to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been deasserted. RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Stop Grant state after initialization until STPCLK# is deasserted. A transition to the Sleep state can be made by the assertion of the SLP# signal.

While in the Stop Grant state, assertions of FLUSH#, SMI#, INIT#, INTR, and NMI will be latched by the processor. These latched events will not be serviced until the processor returns to the Normal state. Only one of each event will be recognized upon return to the Normal state.

2.2.5 Quick Start State

This is a mode entered by the processor with the assertion of the STPCLK# signal when it is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state the

processor is only capable of acting on snoop transactions generated by the system bus priority device. Because of its snooping behavior, Quick Start can only be used in a Uniprocessor (UP) configuration.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters or responding to FLUSH# or BINIT# assertions. While the processor is in the Quick Start state, it will not respond properly to any input signal other than STPCLK#, RESET#, or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

2.2.6 Halt/Grant Snoop State

The processor will respond to snoop transactions on the system bus while in the Auto Halt, Stop Grant or Quick Start state. When a snoop transaction is presented on the system bus the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop has been serviced and the system bus is quiet. After the snoop has been serviced, the processor will return to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state, except for those signal transitions that are required to perform the snoop.

2.2.7 Sleep State

The Sleep state is a very low-power state in which the processor maintains its context and the phase-locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state, the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# signal is not recognized in the Normal or Auto Halt states.

The processor can be reset by the RESET# signal while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly initializes itself.

Input signals (other than RESET#) may not change while the processor is in the Sleep state or transitioning into or out of the Sleep state. Input signal changes at these times will cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state.

While in the Sleep state, the processor can enter its lowest power state, the Deep Sleep state. Removing the processor's input clock puts the processor in the Deep Sleep state. PICCLK may be removed in the Sleep state.

2.2.8 Deep Sleep State

The Deep Sleep state is the lowest power mode the processor can enter while maintaining its context. The Deep Sleep state is entered by stopping the BCLK input to the processor while it is in the Sleep or Quick Start state. For proper operation, the BCLK input should be stopped in the low state.

The processor will return to the Sleep or Quick Start state from the Deep Sleep state when the BCLK input is restarted. Due to the PLL lock latency, there is a 30-µsec delay after the clocks have started before this state transition happens.

PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on when transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion will result in unpredictable behavior.

2.2.9 Operating System Implications of Quick Start and Sleep States

There are a number of architectural features of the Mobile Intel Celeron processor that are not available when the Quick Start state is enabled or do not function in the Quick Start or Sleep state as they do in the Stop Grant state. These features are part of the APIC, time-stamp counter and performance monitor counters. The time-stamp counter and the performance monitor counters are not guaranteed to count in the Quick Start or Sleep states.

2.3 Low Power GTL+

The mobile Intel Celeron processor system bus signals use a variation of the low voltage swing GTL signaling technology. The mobile Intel Celeron processor system bus specification is similar to the Pentium® II processor system bus specification, which is itself a version of GTL with enhanced noise margins and less ringing. The mobile Intel Celeron processor system bus specification reduces system cost and power consumption by raising the termination voltage and termination resistance and changing the termination from dual ended to single ended. Because the specification is different from the standard GTL specification and from the Pentium II processor GTL+ specification, it is referred to as Low Power GTL+.

The Pentium II processor GTL+ system bus depends on incident wave switching and uses flight time for timing calculations of the GTL+ signals. The Low Power GTL+ system bus is short and lightly loaded. With Low Power GTL+ signals, timing calculations are based on capacitive derating. Analog signal simulation of the system bus including trace lengths is highly recommended to ensure that there are no significant transmission line affects. Contact your field sales representative to receive the IBIS models for the mobile Intel Celeron processor.

The GTL+ system bus of the Pentium II processor was designed to support high-speed data transfers with multiple loads on a long bus that behaves like a transmission line. However, in a mobile system, the system bus only has two loads (the processor and the chipset) and the bus traces are short enough that transmission line effects are not significant. It is possible to change the layout and termination of the system bus to take advantage of the mobile environment using the same GTL+ I/O buffers. The benefit is that it reduces the number of terminating resistors in half and substantially reduces the AC and DC power dissipation of the system bus. Low Power GTL+ uses GTL+ I/O buffers but only two loads are allowed. The trace length is limited and the bus is terminated at one end only. Since the system bus is small and lightly loaded, it behaves like a capacitor, and the GTL+ I/O buffers behave like high-speed open-drain buffers. With a 66-MHz bus frequency, the pull-up would be 120Ω. V_{TT} has been increased from 1.5V to processor V_{CC} to eliminate the need for a 1.5V power plane. If 100Ω termination resistors are used rather than 120Ω, then 20% more power will be dissipated in the termination resistors. Intel recommends 120-Ω termination to conserve power.

Refer to the *Mobile Pentium® II Processor System Bus Layout Guideline* (Order Number 243672-001) for details on laying out the Low Power GTL+ system bus.

2.3.1 GTL+ Signals

Two signals of the system bus potentially may not meet the Low Power GTL+ layout requirements: PRDY# and RESET#. These two signals connect to the debug port and might not meet the maximum length requirements. If PRDY# or RESET# do not

meet the layout requirements for Low Power GTL+, then they must be terminated using dual-ended termination at 120Ω. Higher resistor values can be used if simulations show that the signal quality specifications in Section 4 are met.

2.4 Mobile Intel Celeron Processor CPUID

The mobile Intel Celeron processor has the same CPUID family and model number as some Pentium II processors. The mobile Intel Celeron processor can be distinguished from these Pentium II processors by looking at the stepping number and the CPUID cache descriptor information. A mobile Intel Celeron processor has a stepping number in the range of 0AH to 0CH and an L2 cache descriptor of 041H (128-Kbyte L2 cache). If the L2 cache descriptor is 042H, then the processor is a Pentium II processor. The L2 cache must be properly initialized for the L2 cache descriptor information to be correct. After a power-on RESET or when the CPUID version information is loaded, the EAX register contains the values shown in Table 2.4. After the L2 cache is initialized, the CPUID cache/TLB descriptors will be the values shown in Table 2.5.

Table 2.4 Mobile Intel Celeron Processor CPUID

Reserved [31:14]	Type [13:12]	Family [11:8]	Model [7:4]	Stepping [3:0]
X	0	6	6	A - C

Table 2.5 Mobile Intel Celeron Processor CPUID Cache and TLB Descriptors

Cache and TLB Descriptors	01H, 02H, 03H, 04H, 08H, 0CH, 41H

3. ELECTRICAL SPECIFICATIONS

3.1 Processor System Signals

Table 3.1 lists the processor system signals by type.

All Low Power GTL+ signals are synchronous with the BCLK signal. All TAP signals are synchronous with the TCK signal except TRST#. All CMOS input signals can be applied asynchronously.

Table 3.1 System Signal Groups

Group Name	Signals
Low Power GTL+ Input	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
Low Power GTL+ Output	PRDY#
Low Power GTL+ I/O	A[35:3]#, ADS#, AERR#[1], AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BREQ0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
CMOS Input [2, 3]	A20M#, BSEL, FLUSH#, IGNNE#, INIT#, INTR, NMI, PREQ#, PWRGOOD, SLP#, SMI#, STPCLK#
Open Drain Output [3]	FERR#, IERR#
Clock [3]	BCLK
APIC Clock [3]	PICCLK
APIC I/O [3]	PICD[1:0]
Thermal Diode	THERMDA, THERMDC
TAP Input [3]	TCK, TDI, TMS, TRST#
TAP Output [3]	TDO
Power/Other [4]	EDGECTRLN, NC, PLL1, PLL2, TESTHI, TESTHI2, TESTHI3, TESTLO, V_{CC}, V_{CCP}, V_{REF}, V_{SS}

NOTES:

1. The AERR# processor bus pin is removed as a processor feature for mobile Intel Celeron processor at 400MHz and above. The pin must still be terminated to Vcc through a 120Ω pull-up resistor. But the processor must not be configured to drive or observe the pin.
2. See Section 8.1 for information on the PWRGOOD signal.
3. These signals are tolerant to 2.5V only. See Table 3.2 for the recommended pull-up resistor.

4. V_{CC} is the power supply for the core logic; PLL1 and PLL2 are the power supply for the PLL analog section; V_{CCP} is the power supply for the CMOS voltage references; V_{REF} is the voltage reference for the Low Power GTL+ input buffers; V_{SS} is system ground.

Table 3.2 Recommended Resistors for Open-drain Signals

Recommended Resistor Value (W)	Open-drain Signal [1]
150 pull-up	TDI, TDO
680 pull-up	STPCLK#
1K pull-up	INIT#, TCK, TESTHI, TESTHI2, TESTHI3, TMS
680 - 1K pull-down	TRST#
4.7K pull-up	A20M#, FERR#, FLUSH#, IERR#, IGNNE#, INTR, NMI, PREQ#, PWRGOOD, SLP#, SMI#

NOTE:

1. Refer to Section 3.1.4 for the required pull-up or pull-down resistors for signals that are not being used.

The CMOS, Clock, APIC, and TAP inputs can be driven from ground to 2.5V. The TAP outputs are open drain and should be pulled up to 2.5V using resistors with the values shown in Table 3.2. If open-drain drivers are used for input signals, then they should also be pulled up to 2.5V using resistors with the values shown in Table 3.2.

3.1.1 Power Sequencing Requirements

The mobile Intel Celeron processor has no power sequencing requirements. Intel recommends that all of the processor power planes rise to their specified values within one second of each other.

The V_{CC} power plane must not rise too fast. At least 200 µsec (T_R) must pass from the time that V_{CC} is at 10% of its nominal value until the time that V_{CC} is at 90% of its nominal value (see Figure 3.2).

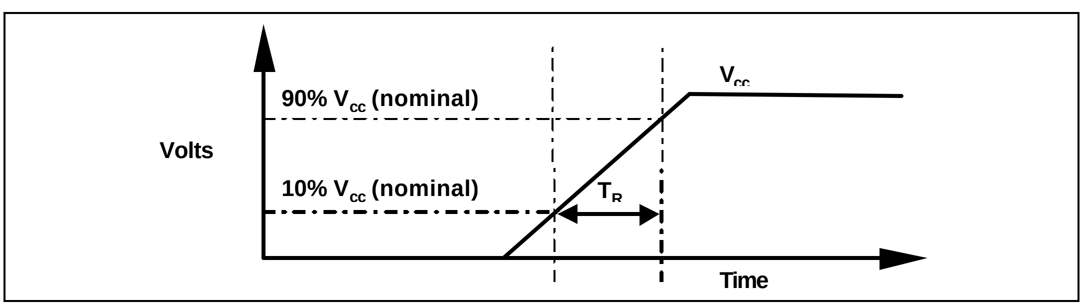


Figure 3.1 Ramp Rate Requirement

3.1.2 Test Access Port (TAP) Connection

The TAP interface is an implementation of the IEEE 1149.1 ("JTAG") standard. Due to the voltage levels supported by the TAP interface, Intel recommends that the mobile Intel Celeron processor and the other 2.5V JTAG specification compliant devices be last in the JTAG chain after any devices with 3.3V or 5.0V JTAG interfaces within the system. A translation buffer should be used to reduce the TDO output voltage of the last 3.3/5.0V device down to the 2.5V range that the mobile Intel Celeron processor can tolerate. Multiple copies of TCK, TMS, and TRST# must be provided—one for each voltage level.

A Debug Port and connector may be placed at the start and end of the JTAG chain containing the processor, with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. There are no requirements for placement of the mobile Intel Celeron processor in the JTAG chain, except for those that are dictated by voltage requirements of the TAP signals.

3.1.3 Catastrophic Thermal Protection

The mobile Intel Celeron processor does not support catastrophic thermal protection or the THERMTRIP# signal. An external thermal sensor should use the thermal diode to protect the processor and the system against excessive temperatures.

3.1.4 Unused Signals

All signals named NC must be unconnected. All signals named TESTLO must be pulled down to V_{SS} or tied directly to V_{SS}. All signals named TESTHI or TESTHI3 must be pulled up to V_{CC} with a resistor. All signals named TESTHI2 must be pulled up to V_{CCP} with a resistor. Each TESTHI and TESTHI2 signal must have an individual, 1kΩ pull-up resistor. The TESTHI3 signals can share a single 1kΩ pull-up.

Unused Low Power GTL+ inputs, outputs, and bi-directional signals should be individually connected to V_{CC} with 120Ω pull-up resistors. Unused CMOS active low inputs should be connected to 2.5V and unused active high inputs should be connected to V_{SS}. Unused open-drain outputs should be unconnected. If the processor is configured to enter the Quick Start state rather than the Stop Grant state, then the SLP# signal should be connected to 2.5V. When tying any signal to power or ground, a resistor will allow for system testability. For unused signals, Intel suggests that 10-kΩ resistors be used for pull-ups and 1-kΩ resistors be used for pull-downs.

PICCLK and PICD[1:0] must be tied to V_{SS} with a 1-kΩ resistor. BSEL must be connected to V_{SS}.

3.1.5 Signal State in Low Power States

3.1.5.1 System Bus Signals

All of the system bus signals have Low Power GTL+ input, output, or input/output drivers. Except when servicing snoops, the system bus signals are tri-stated and pulled up by the termination resistors. Snoops are not permitted in the Sleep and Deep Sleep states.

3.1.5.2 CMOS and Open-drain Signals

The CMOS input signals are allowed to be in either the logic high or low state when the processor is in a low power state. In the Auto Halt and Stop Grant states these signals are allowed to toggle. These input buffers have no internal pull-up or pull-down resistors and system logic can use CMOS or open-drain drivers to drive them.

The open-drain output signals have open-drain drivers and external pull-up resistors are required. One of the two output signals (IERR#) is a catastrophic error indicator and is tri-stated (and pulled-up) when the processor is functioning normally. The FERR# output can be either tri-stated or driven to V_{SS} when the processor is in a low power state depending on the condition of the floating point unit. Since this signal is a DC current path when it is driven to V_{SS}, Intel recommends that the software clear or mask any floating point error condition before putting the processor into the Deep Sleep state.

3.1.5.3 Other Signals

The system bus clock (BCLK) must be driven in all of the low-power states except the Deep Sleep state.

3.2 Power Supply Requirements

3.2.1 Decoupling Recommendations

The amount of bulk decoupling required to meet the processor voltage tolerance requirements is a strong function of the power supply design. Contact your Intel Field Sales Representative for tools to help determine how much decoupling is required. The processor core power plane (V_{CC}) should have at least twenty-six 0.1 µF high frequency decoupling capacitors. The CMOS voltage reference power plane (V_{CCP}) requires 50 µF to 100 µF of bulk decoupling and at least eight 0.1 µF high frequency decoupling capacitors.

For the Low Power GTL+ pull-up resistors, one 0.1 µF high frequency decoupling capacitor is recommended per resistor pack. There should be no more than eight pull-up resistors per resistor pack. The Low Power GTL+ voltage reference power plane (V_{REF}) should have at least three 0.1 µF high frequency decoupling capacitors.

3.2.2 Voltage Planes

All V_{CC} and V_{SS} balls must be connected to the appropriate voltage plane. All V_{CCP} and V_{REF} balls must be connected to the appropriate traces on the system electronics.

In addition to the main V_{CC}, V_{CCP}, and V_{SS} power supply signals, PLL1 and PLL2 provide isolated power to the PLL section. PLL1 and PLL2 should be connected according to Figure 3.2. Do not connect PLL2 directly to V_{SS}. Table 3.3 contains the requirements for C1 and L1.

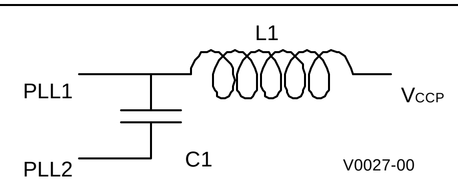


Figure 3.2 PLL LC Filter

Table 3.3 LC Filter Specifications

Symbol	Parameter	Min	Max	Unit	Notes
C1	LC Filter Capacitance	47		µF	≤30% tolerance, 1Ω max series

Table 3.3 LC Filter Specifications

Symbol	Parameter	Min	Max	Unit	Notes
					resistance, ~2 nH series inductance
L1	LC Filter Inductance	20	47	µH	low-Q type choke, ≤30% tolerance, 1.5Ω max series resistance, ≥50 mA current, self-resonant frequency >10 MHz

3.3 System Bus Clock and Processor Clocking

The 2.5-V BCLK clock input directly controls the operating speed of the system bus interface. All system bus timing parameters are specified with respect to the rising edge of the BCLK input. The mobile Intel Celeron processor core frequency is a multiple of the BCLK frequency.

Processors at marked core frequency of 400 MHz and above are implemented with *Bus Fraction Locking* scheme. The Bus Fraction Locking scheme allows the processors to operate at the marked frequency only. In this case, the bus ratio configuration signals are not effective.

Processors with marked core frequency at 366 MHz and below are implemented with *Bus Fraction Limiting* scheme. The processor core frequency must be configured during Reset by using the A20M#, IGNNE#, NMI, and INTR pins (see Table 3.4). The value on these pins during Reset determines the multiplier that the PLL will use for the internal core clock. See the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the definition of these pins during Reset and the operation of the pins after Reset.

Table 3.4 Core Frequency to System Bus Ratio Configuration

Processor Core Frequency to System Bus Frequency Ratio	NMI	INTR	IGNNE#	A20M#	Power-Up Configuration [25:22]
4 (266 MHz)	L	L	L	H	0010
9/2 (300 MHz)	L	H	L	H	0110
5 (333 MHz)	L	L	H	H	0000
11/2 (366 MHz)	L	H	H	H	0100
6 (400 MHz)	H	L	L	L	1011
13/2 (433 MHz)	H	H	L	L	1111
7 (466 MHz)	H	L	H	L	1001

In this case, a multiplexer is required between the system electronics and the processor to drive the bus ratio configuration signals during Reset. Figure 3.6 and Table 3.16 describe the timing requirements for this operation. The 443BX CRESET# signal has suitable timing to control the multiplexer. After RESET# and PWRGOOD are asserted, the multiplexer logic must guarantee that the bus ratio configuration signals encode one of the bus ratios in Table 3.4 and that the bus ratio corresponds to a core frequency at or below the marked core frequency for the processor. The selected bus ratio is visible to software in the Power-On Configuration register, see Section 7.2 for details. The 440MX PCISet contains a multiplexer that meets the requirements described above.

Multiplying the bus clock frequency is necessary to increase performance while allowing for easier distribution of signals within the system. Clock multiplication within the processor is provided by the internal Phase Lock Loop (PLL), which requires a constant frequency BCLK input. During Reset or on exit from the Deep Sleep state, the PLL requires some amount of time to acquire the phase of BCLK. This time is called the PLL lock latency, which is specified in Section 3.6. The system bus frequency ratio can be changed when RESET# is active, assuming that all Reset specifications are met. The BCLK frequency should not be changed during Deep Sleep state (see Section 2.2.8).

3.4 Maximum Ratings

Table 3.5 contains the mobile Intel Celeron processor stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are provided in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 3.5 Mobile Intel Celeron Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{Storage}$	Storage Temperature	–40	85	°C	Note 1
V_{CC}(Abs)	Supply Voltage with respect to V_{SS}	–0.5	3.0	V	
V_{CCP}	CMOS Reference Voltage with respect to V_{SS}	–0.3	3.0	V	
V_{IN}	GTL+ Buffer DC Input Voltage with respect to V_{SS}	–0.3	V_{CC} + 0.7	V	Note 2
V_{IN25}	2.5V Buffer DC Input Voltage with respect to V_{SS}	–0.3	3.3	V	Note 3

NOTES:

1. The shipping container is only rated for 65°C.
2. Parameter applies to the Low Power GTL+ signal groups only.
3. Parameter applies to CMOS, Open-Drain, APIC, and TAP bus signal groups only.

3.5 DC Specifications

Table 3.6 through Table 3.11 list the DC specifications for the mobile Intel Celeron processor.

Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 3.6 Mobile Intel Celeron Processor Power Specifications[1]

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ±135 mV; V_{CCP} = 1.8V ±90 mV						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
V_{CC}	Vcc of core logic	1.765	1.900	2.035	V	±135 mV
$V_{CC,LP}$	V_{CC} when I_{CC} < 300 mA	1.765	1.900	2.105	V	+205/-135 mV [2]
V_{CCP}	V_{CC} for CMOS voltage references	1.710	1.800	1.890	V	1.8V ±90 mV
I_{CC}	I_{CC} for V_{CC} at core frequency at 466 MHz at 433 MHz			12.30 11.50	A A	Note 5
I_{CCP}	Current for V_{CCP}			75	mA	Notes 3, 4, 5
$I_{CC,SG}$	Processor Stop Grant and Auto Halt current			1.70	A	Note 5
$I_{CC,QS}$	Processor Quick Start and Sleep current			1.30	A	Note 5
$I_{CC,DSLP}$	Processor Deep Sleep leakage current			0.65	A	Note 5
dI_{CC}/dt	V_{CC} power supply current slew rate			20	A/µs	Notes 6, 7

NOTES:

1. Specifications in this table apply to the listed frequencies.
2. A higher $V_{CC,MAX}$ is allowed when the processor is in a low power state to enable high efficiency, low current modes in the power regulator.
3. I_{CCP} is the current supply for the CMOS voltage references.
4. Not 100% tested. Specified by design/characterization.
5. $I_{CCx,max}$ specifications are specified at $V_{CC,max}$, $V_{CCP,max}$, and 100°C and under maximum signal loading conditions. $I_{CCx,max}$ specifications are not specified at $V_{CC,LP,max}$ if that voltage specification is used then slightly higher currents can be expected.
6. Based on simulations and averaged over the duration of any change in current. Use to compute the maximum inductance and reaction time of the voltage regulator. This parameter is not tested.
7. Maximum values specified by design/characterization at nominal V_{CC} and V_{CCP}.

Table 3.7 Mobile Intel Celeron Processor Power Specifications[1]

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.6V ±135 mV; V_{CCP} = 1.8V ±90 mV						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
V_{CC}	V_{CC} of core logic for regular voltage processors	1.465	1.600	1.735	V	±135 mV
$V_{CC,LP}$	V_{CC} when I_{CC} < 300 mA	1.465	1.600	1.805	V	+205/-135 mV [2]
V_{CCP}	V_{CC} for CMOS voltage references	1.710	1.800	1.890	V	1.8V ±90 mV
I_{CC}	I_{CC} for V_{CC} at core frequency at 400 MHz at 366 MHz at 333 MHz at 300 MHz at 266 MHz			9.70 8.80 7.95 7.49 6.63	A A A A A	Note 5
I_{CCP}	Current for V_{CCP}			75	mA	Notes 3, 4, 5
$I_{CC,SG}$	Processor Stop Grant and Auto Halt current			1190	mA	Note 5
$I_{CC,QS}$	Processor Quick Start and Sleep current			880	mA	Note 5
$I_{CC,DSLP}$	Processor Deep Sleep leakage current			650	mA	Note 5
dI_{CC}/dt	V_{CC} power supply current slew rate			20	A/µs	Notes 6, 7

NOTES:

1. Specifications in this table apply to the listed frequencies.
2. A higher $V_{CC,MAX}$ is allowed when the processor is in a low power state to enable high efficiency, low current modes in the power regulator.
3. I_{CCP} is the current supply for the CMOS voltage references.
4. Not 100% tested. Specified by design/characterization.
5. $I_{CCx,max}$ specifications are specified at $V_{CC,max}$, $V_{CCP,max}$, and 100°C and under maximum signal loading conditions. $I_{CCx,max}$ specifications are not specified at $V_{CC,LP,max}$ if that voltage specification is used then slightly higher currents can be expected.
6. Based on simulations and averaged over the duration of any change in current. Use to compute the maximum inductance and reaction time of the voltage regulator. This parameter is not tested.
7. Maximum values specified by design/characterization at nominal V_{CC} and V_{CCP}.

Table 3.8 Low Voltage Mobile Intel Celeron Processor Power Specifications[1]

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.5V ±135 mV; V_{CCP} = 1.8V ±90 mV						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
V_{CC}	Vcc of core logic for 266PE MHz at low voltage	1.365	1.500	1.635	V	±135 mV
$V_{CC,LP}$	V_{CC} when I_{CC} < 300 mA	1.365	1.500	1.705	V	+205/-135 mV [2]
V_{CCP}	V_{CC} for CMOS voltage references	1.710	1.800	1.890	V	1.8V ±90 mV
I_{CC}	I_{CC} for V_{CC} at 266 MHz at core frequency			5.90	A	Note 5
I_{CCP}	Current for V_{CCP}			75	mA	Notes 3, 4, 5
$I_{CC,SG}$	Processor Stop Grant and Auto Halt current			940	mA	Note 5
$I_{CC,QS}$	Processor Quick Start and Sleep current			630	mA	Note 5
$I_{CC,DSLP}$	Processor Deep Sleep leakage current			400	mA	Note 5
dI_{CC}/dt	V_{CC} power supply current slew rate			20	A/µs	Notes 6, 7

NOTES:

1. Specifications in this table apply to the listed frequency.
2. A higher $V_{CC,MAX}$ is allowed when the processor is in a low-power state to enable high efficiency, low-current modes in the power regulator.
3. I_{CCP} is the current supply for the CMOS voltage references.
4. Not 100% tested. Specified by design/characterization.
5. $I_{CCx,max}$ specifications are specified at $V_{CC,max}$, $V_{CCP,max}$, and 100°C and under maximum signal loading conditions. $I_{CCx,max}$ specifications are not specified at $V_{CC,LP,max}$ if that voltage specification is used then slightly higher currents can be expected.
6. Based on simulations and averaged over the duration of any change in current. Use to compute the maximum inductance and reaction time of the voltage regulator. This parameter is not tested.
7. Maximum values specified by design/characterization at nominal V_{CC} and V_{CCP}.

The signals on the mobile Intel Celeron processor system bus are included in the Low Power GTL+ signal group. These signals are specified to be terminated to V_{CC}. The DC specifications for these

signals are listed in Table 3.9; the termination and reference voltage specifications for these signals are listed in Table 3.10. The mobile Intel Celeron processor requires external termination and a V_{REF}. Refer to *Mobile Pentium® II Processor System Bus Layout Guideline* (Order Number 243672-001) for full details of system V_{TT} and V_{REF} requirements.

Table 3.9 Low Power GTL+ Signal Group DC Specifications

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	–0.3	$^5/_9 V_{TT}$ – 0.2	V	See Table 3.10 [1]
V_{IH}	Input High Voltage	$^5/_9 V_{TT}$ + 0.2	V_{CC}	V	Note 1
V_{OH}	Output High Voltage	—	—	V	See V_{TT} max in Table 3.10.
R_{ON}	Output Low Drive Strength		35	ohms	
I_L	Leakage Current		±100	µA	Note 2
I_{LO}	Output Leakage Current		±30	µA	Note 3

NOTES:

1. V_{REF} worst case, not nominal. Noise on V_{REF} should be accounted for.
2. $(0 \le V_{IN} \le V_{CC})$.
3. $(0 \le V_{OUT} \le V_{CC})$.

Table 3.10. Low Power GTL+ Bus DC Specifications

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
V_{TT}	Bus Termination Voltage	$V_{CC,MIN}$	V_{CC}	$V_{CC,MAX}$	V	Note 1
V_{REF}	Input Reference Voltage	$^5/_9 V_{TT}$ – 2%	$^5/_9 V_{TT}$	$^5/_9 V_{TT}$ + 2%	V	±2% [2]

NOTES:

1. The intent is to use the same power supply for V_{CC} and V_{TT}.
2. V_{REF} for the system logic should be created from V_{TT} by a voltage divider.

Table 3.11 Clock, APIC, TAP, CMOS and Open-Drain Signal Group DC Specifications

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	–0.3	0.7	V	
$V_{IL,BCLK}$	Input Low Voltage, BCLK	–0.3	0.7	V	
V_{IH}	Input High Voltage	1.7	2.625	V	
$V_{IH,BCLK}$	Input High Voltage, BCLK	1.8	2.625	V	
V_{OL}	Output Low Voltage		0.4	V	Note 1
V_{OH}	Output High Voltage	N/A	2.625	V	All outputs are open-drain
I_{OL}	Output Low Current		14	mA	
I_{LI}	Input Leakage Current		±100	µA	Note 2
I_{LO}	Output Leakage Current		±30	µA	Note 2

NOTES:

1. Parameter measured at 14 mA.
2. ($0 \leq V_{IN} \leq 2.625$V).

The Clock, CMOS, Open-drain, and TAP signals are designed to interface at 2.5V CMOS levels to allow connection to other devices. The DC specifications for these 2.5V tolerant signals are listed in Table 3.11.

3.6 AC Specifications

3.6.1 System Bus, Clock, APIC, TAP, CMOS, and Open-drain AC Specifications

Table 3.12 through Table 3.19 provide AC specifications associated with the mobile Intel Celeron processor. The AC specifications are divided into the following categories: Table 3.12 contains the system bus clock specifications; Table 3.13 contains the processor core frequencies; Table 3.14 contains the Low Power GTL+ specifications; Table 3.15 contains the CMOS and Open-Drain signal groups specifications; Table 3.16 contains timings for the reset conditions; Table 3.17 contains the TAP specifications; and Table 3.18 and Table 3.19 contain the power management timing specifications.

All system bus AC specifications for the Low Power GTL+ signal group are relative to the rising edge of the BCLK input at 1.25V. All Low Power GTL+ timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

Table 3.12 System Bus Clock AC Specifications[1]

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
	System Bus Frequency		66.67		MHz		
T1	BCLK Period		15		ns	3.3	Note 2
T2	BCLK Period Stability			±250	ps		Notes 3, 4
T3	BCLK High Time	5.0			ns	3.3	At >1.8V
T4	BCLK Low Time	5.0			ns	3.3	At <0.7V
T5	BCLK Rise Time	0.125		0.875	ns	3.3	(0.9V – 1.6V) [4]
T6	BCLK Fall Time	0.125		0.875	ns	3.3	(1.6V – 0.9V) [4]

NOTES:

1. All AC timings for Low Power GTL+ and CMOS signals are referenced to the BCLK rising edge at 1.25V. All CMOS signals are referenced at 1.25V.
2. The BCLK period allows a +0.5-ns tolerance for clock driver variation.
3. Not 100% tested. Specified by design/characterization.
4. Measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.

Table 3.13 Valid Mobile Intel Celeron Processor Frequencies

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV		
BCLK Frequency (MHz)	**Frequency Multiplier**	**Core Frequency (MHz)**
66.67	4	266.67
66.67	9/2	300.00
66.67	5	333.00
66.67	11/2	366.67
66.67	6	400.00
66.67	13/2	433.00
66.67	7	466.00

NOTE: While other combinations of bus and core frequencies are defined, operation at frequencies other than those listed in Table 3.13 will not be validated by Intel and are not guaranteed. The frequency multiplier is programmed into the processor when it is manufactured and it cannot be changed.

Table 3.14 Low Power GTL+ Signal Groups AC Specifications[1]

R_{TT} = 120Ω terminated to V_{CC}; V_{REF} = 5/9 V_{CC}; load = 0pF T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
T7	Low Power GTL+ Output Valid Delay	0.00	7.78	ns	3.4	
T8	Low Power GTL+ Input Setup Time	2.98		ns	3.5	Notes 2, 3
T9	Low Power GTL+ Input Hold Time	0.90		ns	3.5	Note 4
T10	RESET# Pulse Width	1		ms	3.6, 3.7	Note 5

NOTES:

1. All AC timings for Low Power GTL+ signals are referenced to the BCLK rising edge at 1.25V. All Low Power GTL+ signals are referenced at V_{REF}.
2. RESET# can be asserted (active) asynchronously but must be deasserted synchronously.
3. Specification is for a minimum 0.40V swing.
4. Specification is for a maximum 1.0V swing.
5. After V_{CC}, V_{CCP}, and BCLK become stable and PWRGOOD is asserted.

Table 3.15 CMOS and Open-Drain Signal Groups AC Specifications[1, 2]

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
T14	2.5V Input Pulse Width, except PWRGOOD	2		BCLKs	3.4	Active and Inactive states
T15	PWRGOOD Inactive Pulse Width	10		BCLKs	3.7	Notes 3, 4

NOTES:

1. All AC timings for CMOS and Open-drain signals are referenced to the BCLK rising edge at 1.25V. All CMOS and Open-drain signals are referenced at 1.25V.
2. Minimum output pulse width on CMOS outputs is 2 BCLKs.
3. When driven inactive, or after V_{CC}, $V_{CCP,}$ and BCLK become stable. PWRGOOD must remain below $V_{IL,max}$ from Table 3.11 until all the voltage planes meet the voltage tolerance specifications in Table 3.7, and BCLK has met the BCLK AC specifications in Table 3.12 for at least 10 clock cycles. PWRGOOD must rise error-free and monotonically to 2.5V.
4. If the BCLK signal meets its AC specification within 150 ns of turning on then the PWRGOOD Inactive Pulse Width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the voltage planes meet the voltage tolerance specifications.

Table 3.16 Reset Configuration AC Specifications

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
T16	Reset Configuration Signals (A[15:5]#, BR0#, FLUSH#, INIT#, PICD0) Setup Time	4		BCLKs	3.5, 3.6	Before deassertion of RESET#
T17	Reset Configuration Signals (A[15:5]#, BR0#, FLUSH#, INIT#, PICD0) Hold Time	2	20	BCLKs	3.5, 3.6	After clock that deasserts RESET#
T18	Reset Configuration Signals (A20M#, IGNNE#, INTR, NMI) Setup Time	1		ms	3.7	Before deassertion of RESET#, Note 1
T19	Reset Configuration Signals (A20M#, IGNNE#, INTR, NMI) Delay Time		5	BCLKs	3.7	After assertion of RESET#, Note
T20	Reset Configuration Signals (A20M#, IGNNE#, INTR, NMI) Hold Time	2	20	BCLKs	3.5, 3.7	After clock that deasserts RESET#

NOTES:

1. At least 1 ms must pass after PWRGOOD rises above $V_{IH,min}$ from Table 3.11 and BCLK meets its AC timing specification, until RESET# may be deasserted.
2. For a Reset, the clock ratio defined by these signals must be a safe value (their final value or a lower multiplier) within this delay after RESET# is asserted unless PWRGOOD is inactive (below $V_{IL,max}$).

Table 3.17 TAP Signal AC Specifications[1]

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T30	TCK Frequency	—	16.67	MHz		
T31	TCK Period	60	—	ns	3.3	
T32	TCK High Time	25.0		ns	3.3	≥ 1.7V [2]
T33	TCK Low Time	25.0		ns	3.3	≤ 0.7V [2]
T34	TCK Rise Time		5.0	ns	3.3	(0.7V-1.7V) [2,3]
T35	TCK Fall Time		5.0	ns	3.3	(1.7V-0.7V) [2,3]
T36	TRST# Pulse Width	40.0		ns	3.9	Asynchronous [2]
T37	TDI, TMS Setup Time	5.0		ns	3.8	Note 4
T38	TDI, TMS Hold Time	14.0		ns	3.8	Note 4
T39	TDO Valid Delay	1.0	10.0	ns	3.8	Notes 5, 6
T40	TDO Float Delay		25.0	ns	3.8	Notes 2, 5, 6
T41	All Non-Test Outputs Valid Delay	2.0	25.0	ns	3.8	Notes 5, 7, 8
T42	All Non-Test Outputs Float Delay		25.0	ns	3.8	Notes 2, 5, 7, 8
T43	All Non-Test Inputs Setup Time	5.0		ns	3.8	Notes 4, 7, 8
T44	All Non-Test Inputs Hold Time	13.0		ns	3.8	Notes 4, 7, 8

NOTES:

1. All AC timings for TAP signals are referenced to the TCK rising edge at 1.25V. All CMOS signals are referenced at 1.25V.
2. Not 100% tested. Specified by design/characterization.
3. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16 MHz.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. Valid delay timing for this signal is specified into 150Ω terminated to 2.5V and 0 pF of external load. For real system timings these specifications must be derated for external capacitance at 105 ps/pF.
7. Non-Test Outputs and Inputs are the normal output or input signals (except TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
8. During Debug Port operation use the normal specified timings rather than the TAP signal timings.

Table 3.18 Quick Start/Deep Sleep AC Specifications

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**
T45	Stop Grant Cycle Completion to Clock Stop	100		BCLKs	3.10
T46	Stop Grant Cycle Completion to Input Signals Stable		0	ns	3.10
T47	Deep Sleep PLL Lock Latency		30	µs	3.10
T48	STPCLK# Hold Time from PLL Lock	0		ns	3.10
T49	Input Signal Hold Time from STPCLK# Deassertion	8		BCLKs	3.10

NOTE:

1. Input signals other than RESET# and BPRI# must be held constant in the Quick Start state.

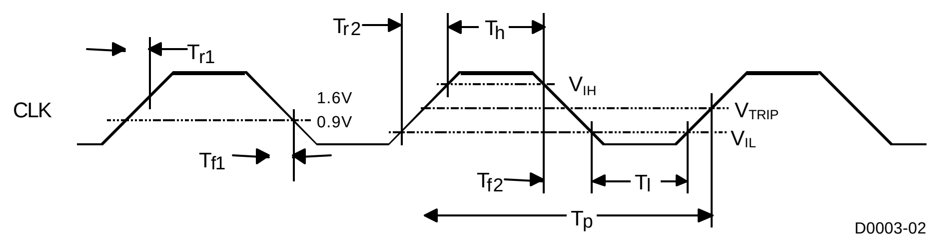
Table 3.19 Stop Grant/Sleep/Deep Sleep AC Specifications

T_{CASE} = 0 to $T_{CASE,max}$; V_{CC} = 1.9V ± 135 mV, 1.6V ± 135 mV, or 1.5V ± 135 mV; V_{CCP} = 1.8V ±90 mV					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**
T50	SLP# Signal Hold Time from Stop Grant Cycle Completion	100		BCLKs	3.11
T51	SLP# Assertion to Input Signals Stable		0	ns	3.11
T52	SLP# Assertion to Clock Stop	10		BCLKs	3.11
T54	SLP# Hold Time from PLL Lock	0		ns	3.11
T55	STPCLK# Hold Time from SLP# Deassertion	10		BCLKs	3.11
T56	Input Signal Hold Time from SLP# Deassertion	10		BCLKs	3.11

NOTE:

1. Input signals other than RESET# must be held constant in the Sleep state.

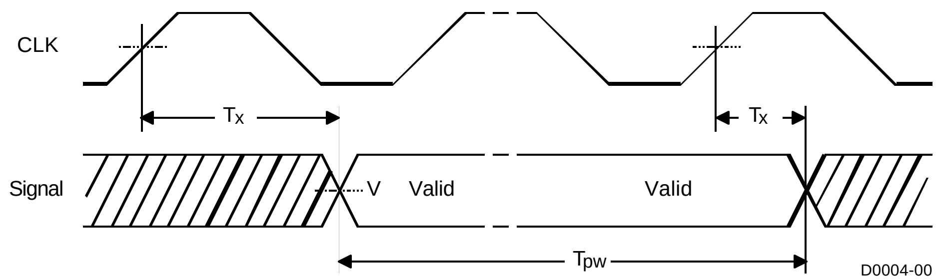
Figure 3.3 through Figure 3.11 are to be used in conjunction with Table 3.12 through Table 3.19.



NOTES:

T_{r1} = T5, T_{r2} = T34 (Rise Time)
T_{f1} = T6, T_{f2} = T35 (Fall Time)
T_h = T3, T32 (High Time)
T_l = T4, T33 (Low Time)
T_p = T1, T31 (Period)

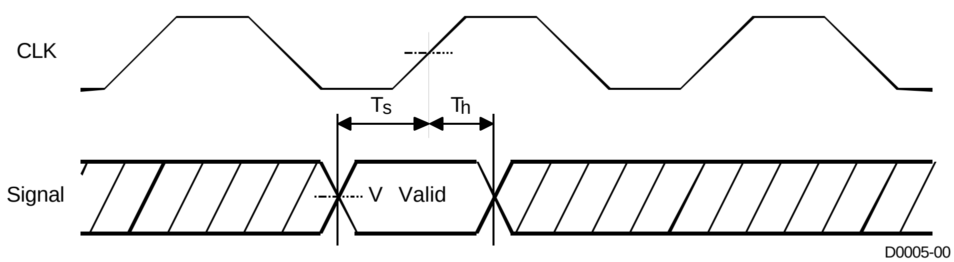
Figure 3.3 Generic Clock Waveform



NOTES:

T_x = T7, T11 (Valid Delay)
T_{pw} = T14 (Pulse Width)
V = V_{REF} for Low Power GTL+ signal group; 1.25V for CMOS, Open-Drain, and TAP signal groups

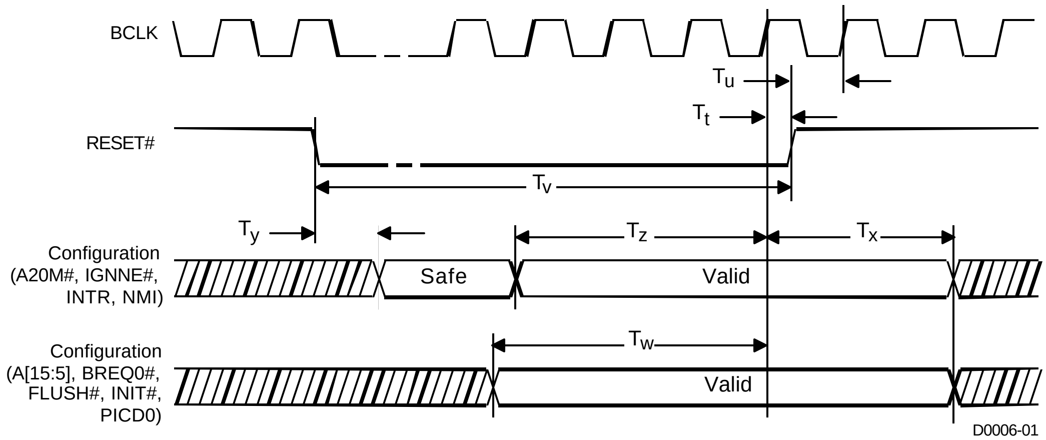
Figure 3.4 Valid Delay Timings



NOTES:

T_s = T8, T12 (Setup Time)
T_h = T9, T13 (Hold Time)
V = V_{REF} for Low Power GTL+ signals; 1.25V for CMOS and TAP signals

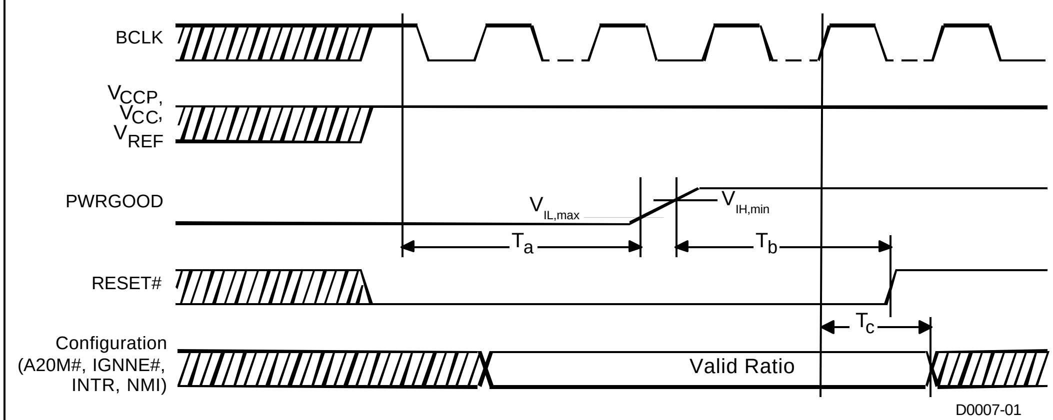
Figure 3.5 Setup and Hold Timings



NOTES:

- T_t = T9 (Low Power GTL+ Input Hold Time)
- T_u = T8 (Low Power GTL+ Input Setup Time)
- T_v = T10 (RESET# Pulse Width)
- T_w = T16 (Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Setup Time)
- T_x = T17 (Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Hold Time)
  T20 (Reset Configuration Signals (A20M#, IGNNE#, INTR, NMI) Hold Time)
- T_y = T19 (Reset Configuration Signals (A20M#, IGNNE#, INTR, NMI) Delay Time)
- T_z = T18 (Reset Configuration Signals (A20M#, IGNNE#, INTR, NMI) Setup Time)

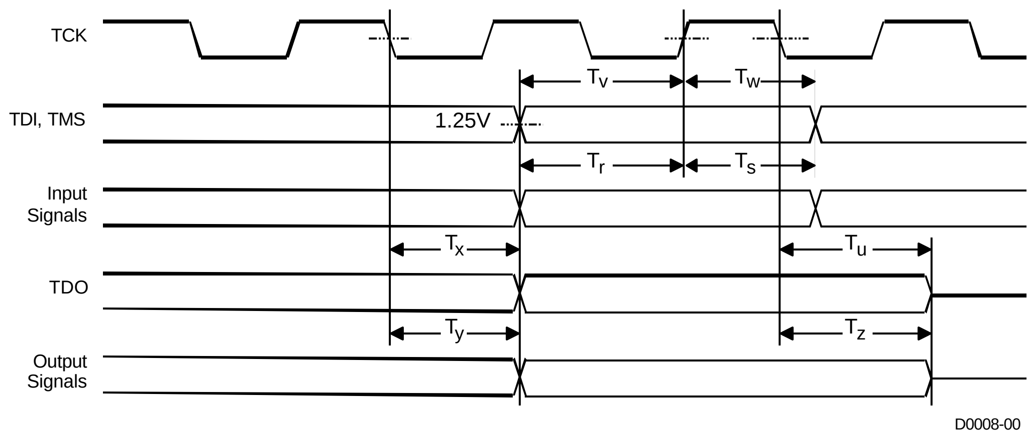
Figure 3.6 Reset and Configuration Timings



NOTES:

T_a = T15 (PWRGOOD Inactive Pulse Width)
T_b = T10 (RESET# Pulse Width)
T_c = T20 (Reset Configuration Signals (A20M#, IGNNE#, INTR, NMI) Hold Time)

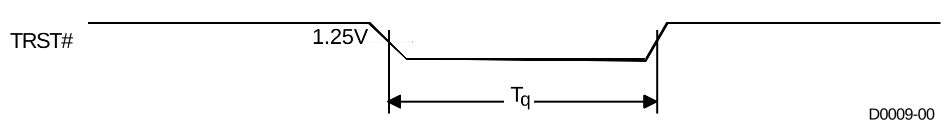
Figure 3.7 Power-on Reset Timings



NOTES:

T_r = T43 (All Non-Test Inputs Setup Time)
T_s = T44 (All Non-Test Inputs Hold Time)
T_u = T40 (TDO Float Delay)
T_v = T37 (TDI, TMS Setup Time)
T_w = T38 (TDI, TMS Hold Time)
T_x = T39 (TDO Valid Delay)
T_y = T41 (All Non-Test Outputs Valid Delay)
T_z = T42 (All Non-Test Outputs Float Delay)

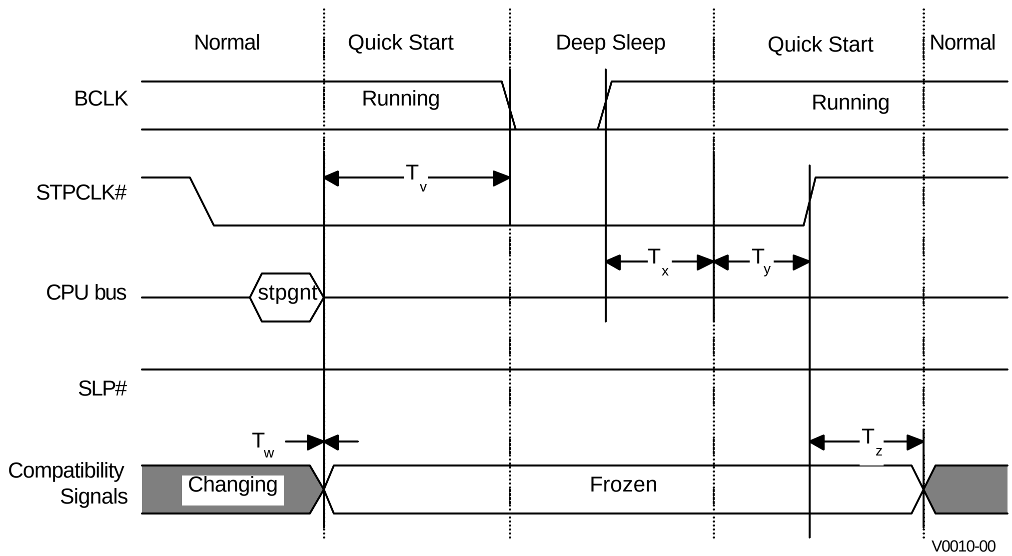
Figure 3.8 Test Timings (Boundary Scan)



NOTE:

T_q = T36 (TRST# Pulse Width)

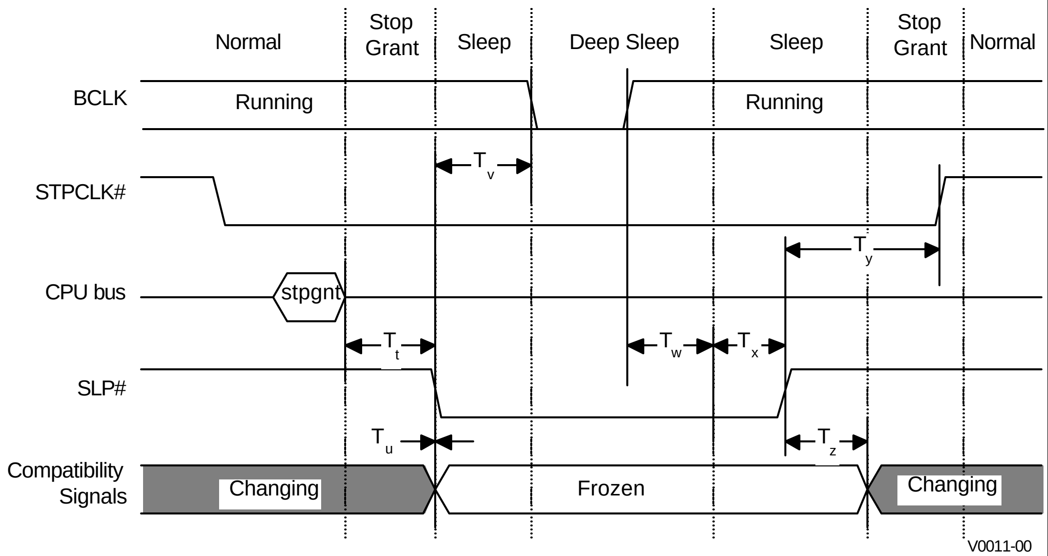
Figure 3.9 Test Reset Timings



NOTES:

T_v = T45 (Stop Grant Acknowledge Bus Cycle Completion to Clock Shut Off Delay)
T_w = T46 (Setup Time to Input Signal Hold Requirement)
T_x = T47 (Deep Sleep PLL Lock Latency)
T_y = T48 (PLL lock to STPCLK# Hold Time)
T_z = T49 (Input Signal Hold Time)

Figure 3.10 Quick Start/Deep Sleep Timing



NOTES:

T_t = T50 (Stop Grant Acknowledge Bus Cycle Completion to SLP# Assertion Delay)
T_u = T51 (Setup Time to Input Signal Hold Requirement)
T_v = T52 (SLP# assertion to clock shut off delay)
T_w = T47 (Deep Sleep PLL lock latency)
T_x = T54 (SLP# Hold Time)
T_y = T55 (STPCLK# Hold Time)
T_z = T56 (Input Signal Hold Time)

Figure 3.11 Stop Grant/Sleep/Deep Sleep Timing

4. SYSTEM SIGNAL SIMULATIONS

Many scenarios have been simulated to generate a set of Low Power GTL+ processor system bus layout guidelines which are available in the *Mobile Pentium® II Processor System Bus Layout Guideline* (Order Number 243672-001). Systems must be simulated using the IBIS model to determine if they are compliant with this specification.

4.1 System Bus Clock (BCLK) Signal Quality Specifications

Table 4.1 and Figure 4.1 show the signal quality for the system bus clock (BCLK) signal at the processor. The timings illustrated in Figure 4.1 are taken from Table 3.12. BCLK is a 2.5-V clock.

Table 4.1 BCLK Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	$V_{IL,BCLK}$		0.7	V	4.1	Note 1
V2	$V_{IH,BCLK}$	1.8		V	4.1	Note 1
V3	V_{IN} Absolute Voltage Range	–0.7	3.5	V	4.1	Undershoot, Overshoot
V4	Rising Edge Ringback	1.8		V	4.1	Absolute Value [2]
V5	Falling Edge Ringback		0.7	V	4.1	Absolute Value [2]

NOTES:

1. BCLK must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,BCLK}$.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the $V_{IH,BCLK}$ (rising) or $V_{IL,BCLK}$ (falling) voltage limits.

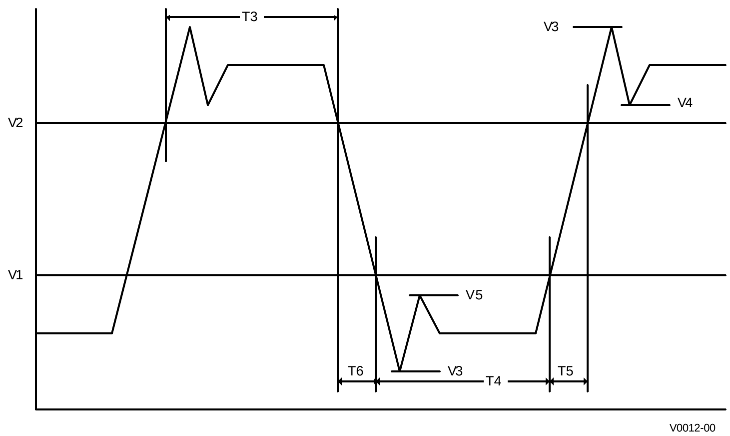


Figure 4.1 BCLK Generic Clock Waveform

4.2 Low Power GTL+ Signal Quality Specifications

Table 4.2 and Figure 4.2 illustrate the Low Power GTL+ signal quality specifications for the mobile Intel Celeron processor. Refer to the *Pentium® II Processor Developer's Manual* for the GTL+ buffer specification.

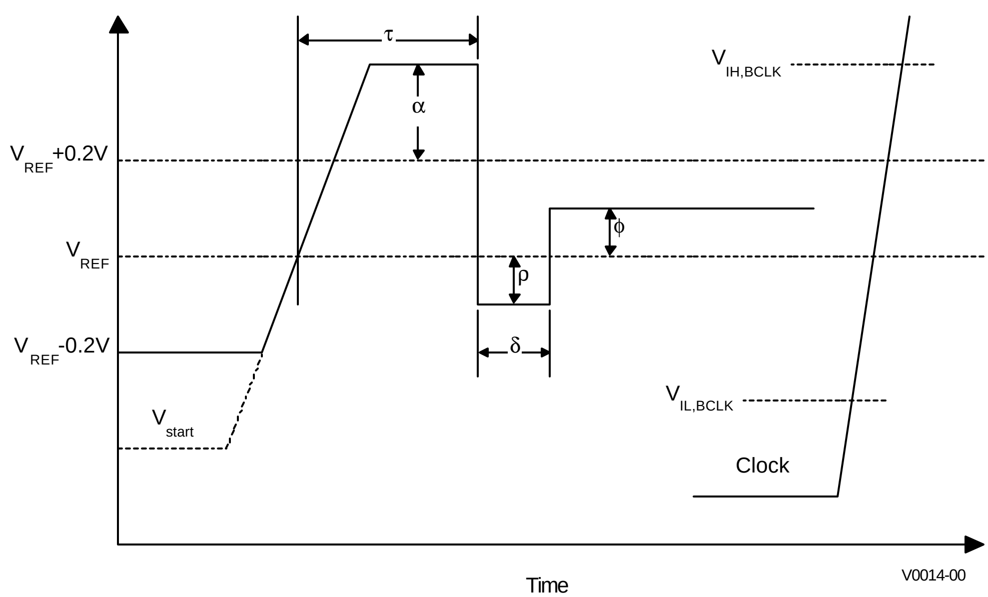
Table 4.2 Low Power GTL+ Signal Group Ringback Specification

Symbol	Parameter	Min	Unit	Figure	Notes
α	Overshoot	100	mV	4.2	Notes 1, 2
τ	Minimum Time at High	1	ns	4.2	Notes 1, 2
ρ	Amplitude of Ringback	-100	mV	4.2	Notes 1, 2, 3
ϕ	Final Settling Voltage	100	mV	4.2	Notes 1, 2
δ	Duration of Sequential Ringback	N/A	ns	4.2	Notes 1, 2

NOTES:

1. Specified for the edge rate of 0.3 – 0.8 V/ns. See Figure 4.2 for the generic waveform.
2. All values determined by design/characterization.

3. Ringback below V_{REF} +100 mV is not authorized during low to high transitions. Ringback above V_{REF} -100mV is not authorized during high to low transitions.



NOTE: High-to-low case is analogous.

Figure 4.2 Low to High, Low Power GTL+ Receiver Ringback Tolerance

4.3 Non-Low Power GTL+ Signal Quality Specifications

Signals driven to the mobile Intel Celeron processor should meet signal quality specifications to ensure that the processor reads data properly and that incoming signals do not affect the long-term reliability of the processor. There are three signal quality parameters defined: overshoot/undershoot, ringback and settling limit. All three signal quality parameters are shown in Figure 4.3 for non-GTL+ signal groups.

4.3.1 Overshoot and Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot/undershoot

guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on 2.5V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough).

However, excessive ringback is the dominant detrimental system timing effect resulting from overshoot/undershoot (for example, violating the overshoot/undershoot guideline will make it difficult to satisfy the ringback specification). The overshoot/undershoot guideline is 0.8V and assumes the absence of diodes on the input. These guidelines should be verified in simulations *without the on-chip ESD protection diodes present* because the diodes will begin clamping the 2.5-V tolerant signals beginning at approximately 1.25V above V_{CC} and 0.5V below V_{SS}. If the signals do not reach the clamping voltage, then this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

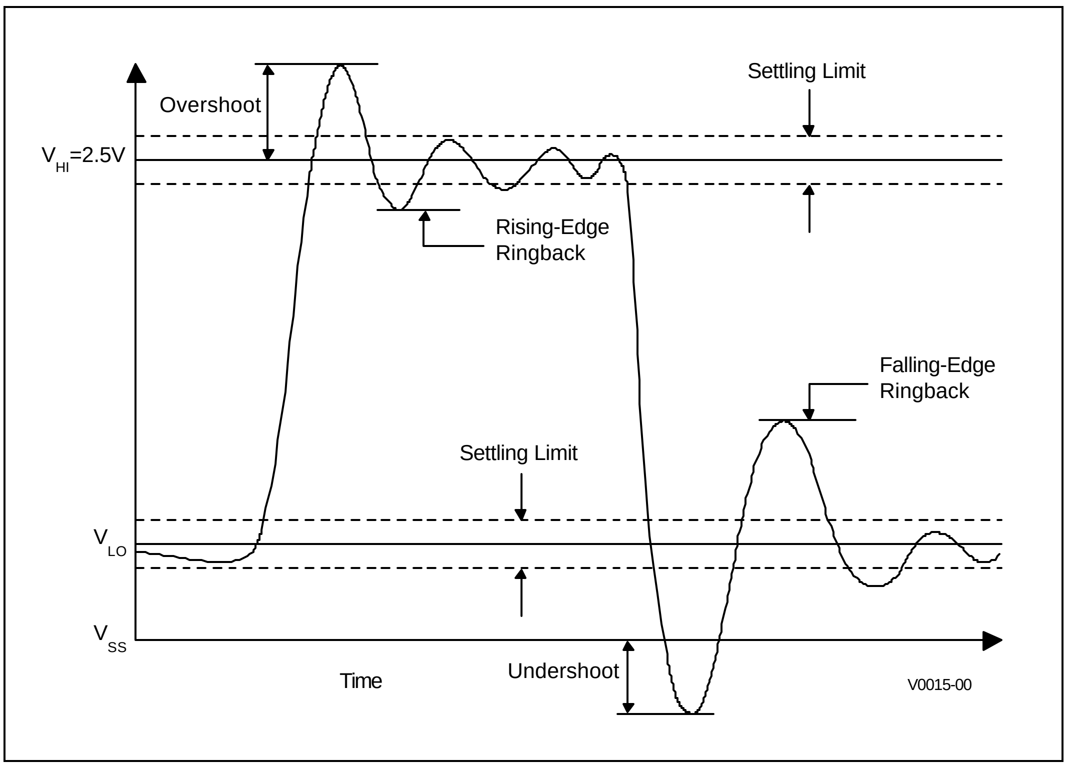


Figure 4.3 Non-GTL+ Overshoot/Undershoot and Ringback

4.3.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is the voltage that the signal rings back to after achieving its maximum absolute value. Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input signal of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for the non-GTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 4.3 for the signal ringback specifications for non-GTL+ signals.

4.3.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving signal that a signal may reach before its next transition. The amount allowed is 10% of the total signal swing ($V_{HI} – V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before its next transition.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations that could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of five to ten successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

Table 4.3 Signal Ringback Specifications for Non-GTL+ Signals

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Figure
Non-GTL+ Signals	$0 \rightarrow 1$	1.7 V	4.3
Non-GTL+ Signals	$1 \rightarrow 0$	0.7 V	4.3

5. MECHANICAL SPECIFICATIONS

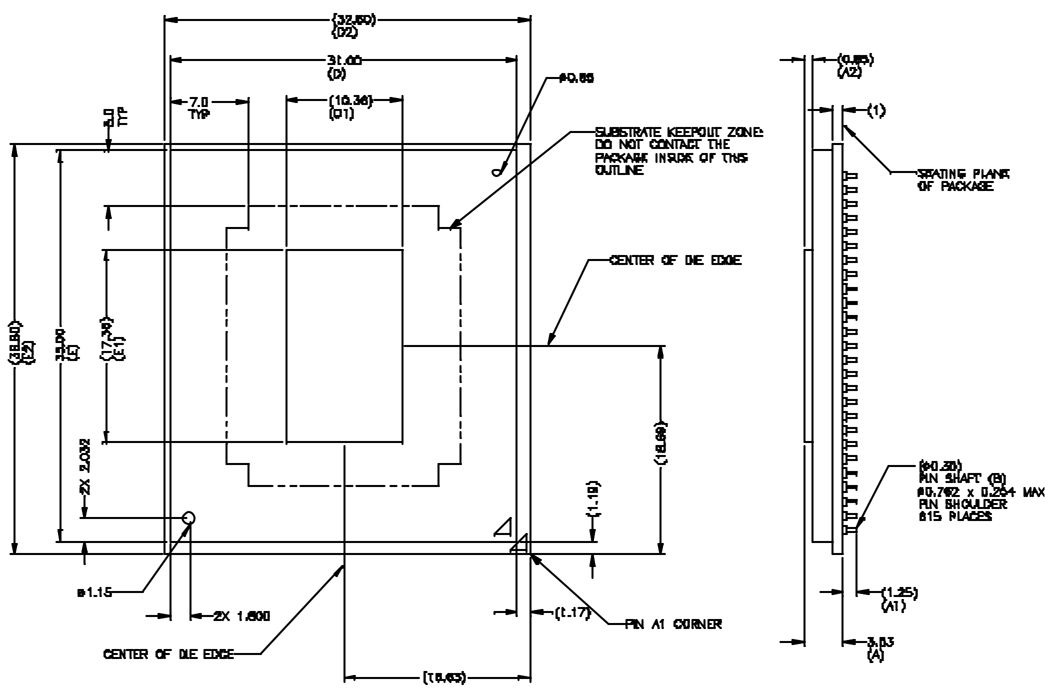
The mobile Intel Celeron processor is packaged in an PPGA-B615 package (also known as Micro-PGA) or an PBGA-B615 package (also known as BGA), with the back of the processor die exposed on top. This section contains information describing the packages and the signal pin assignments.

5.1 Dimensions of the Micro-PGA Package

The mechanical specifications for the Micro-PGA package are provided in Table 5.1 and shown in Figure 5.1 and Figure 5.2.

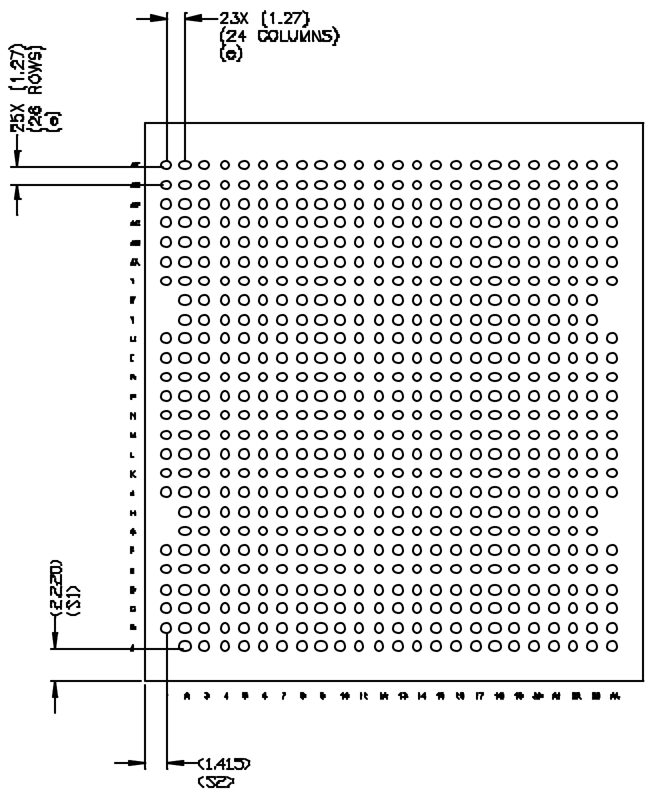
Table 5.1 Micro-PGA Package Mechanical Specifications

Symbol	Parameter	Min	Max	Unit
A	Overall height, top of die to seating plane of the interposer	3.23	3.83	mm
A_1	Pin length	1.25 REF		mm
A_2	Die Height	0.854 REF		mm
B	Pin Diameter	0.30 REF		mm
D	Die Substrate Width	30.85	31.15	mm
D_1	Die Width	10.36 REF		mm
D_2	Package Width	32.60 REF		mm
E	Die Substrate Length	34.85	35.15	mm
E_1	Die Length	17.36 REF		mm
E_2	Package Length	36.80 REF		mm
e	Pin pitch	1.27 REF		mm
—	Pin Tip Radial True Position	<= 0.127		mm
N	Pin Count	615		each
S_1	Pin row A to short edge of interposer	2.220 REF		mm
S_2	Pin column 1 to long edge of interposer	1.415 REF		mm
P_{DIE}	Allowable Pressure on the Die for Thermal Solution	—	689	kPa
W	Package Weight	7.5 REF		gram



NOTE: Dimensions in parentheses are for reference only. All dimensions are in millimeters.

Figure 5.1 Micro-PGA Package-Top and Side View



NOTE: Dimensions in parentheses are for reference only. All dimensions are in millimeters.

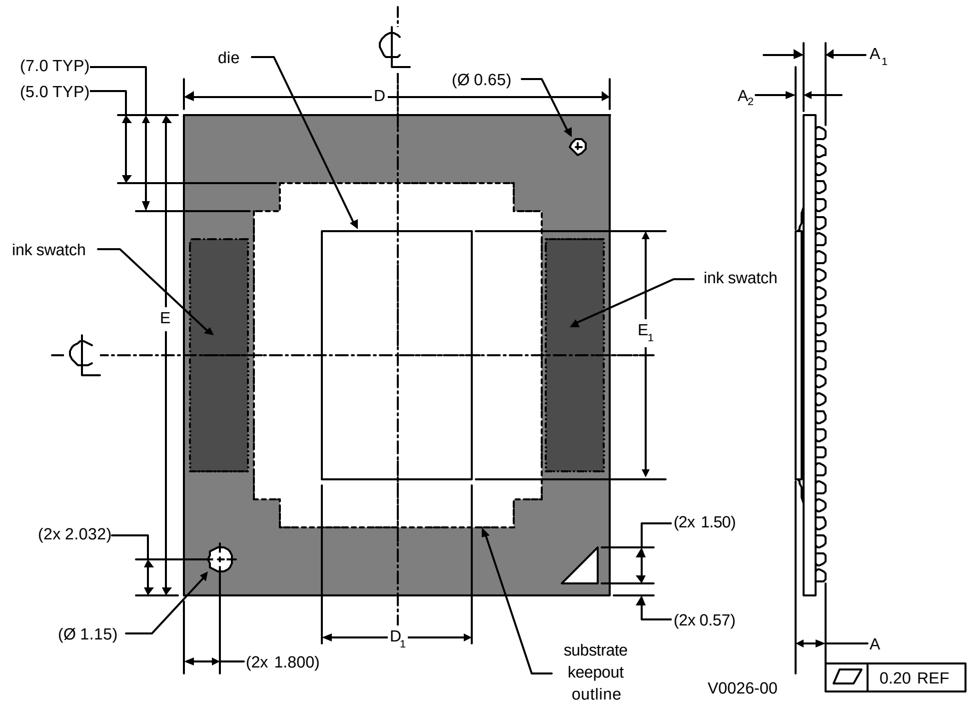
Figure 5.2 Micro-PGA Package-Bottom View

5.2 Dimensions of the BGA Package

The mechanical specifications for the surface-mount BGA package are provided in Table 5.2. Figure 5.3 shows the top and side views of the surface-mount package, and Figure 5.4 shows the bottom view of the surface-mount package. For component handling, the substrate may only be contacted within the shaded region between the keep-out outline and the edge of the substrate.

Table 5.2 Surface-mount BGA Package Specifications

Symbol	Parameter	Min	Max	Unit
A	Overall Height, as delivered	2.29	2.79	mm
A_1	Substrate Height, as delivered	1.50 REF		mm
A_2	Die Height	0.854 REF		mm
B	Ball Diameter	0.78 REF		mm
D	Package Width	30.85	31.15	mm
D_1	Die Width	10.36 REF		mm
E	Package Length	34.85	35.15	mm
e	Ball Pitch	1.27		mm
E_1	Die Length	17.36 REF		mm
N	Ball Count	615		each
S_1	Outer Ball Center to Short Edge of Substrate	1.625 REF		mm
S_2	Outer Ball Center to Long Edge of Substrate	0.895 REF		mm
P_{DIE}	Allowable Pressure on the Die for Thermal Solution	—	689	kPa
W	Package Weight	3.71	4.52	grams



NOTE: Dimensions are for reference only. All dimensions are in millimeters.

Figure 5.3 Surface-mount BGA Package - Top and Side View

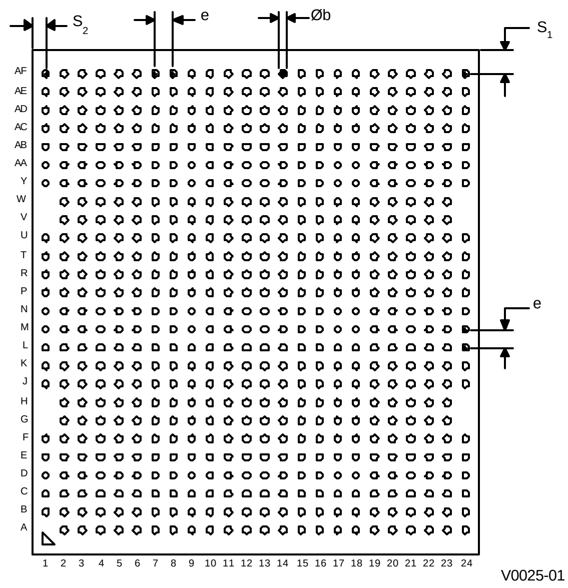


Figure 5.4 Surface-mount BGA Package - Bottom View

5.3 Signal Listings

Figure 5.5 is a topside view of the pin/ball map of the mobile Intel Celeron processor with the voltage balls called out. Table 5.3 lists the signals in pin/ball number order. Table 5.4 and Table 5.5 list the signals in signal name order.

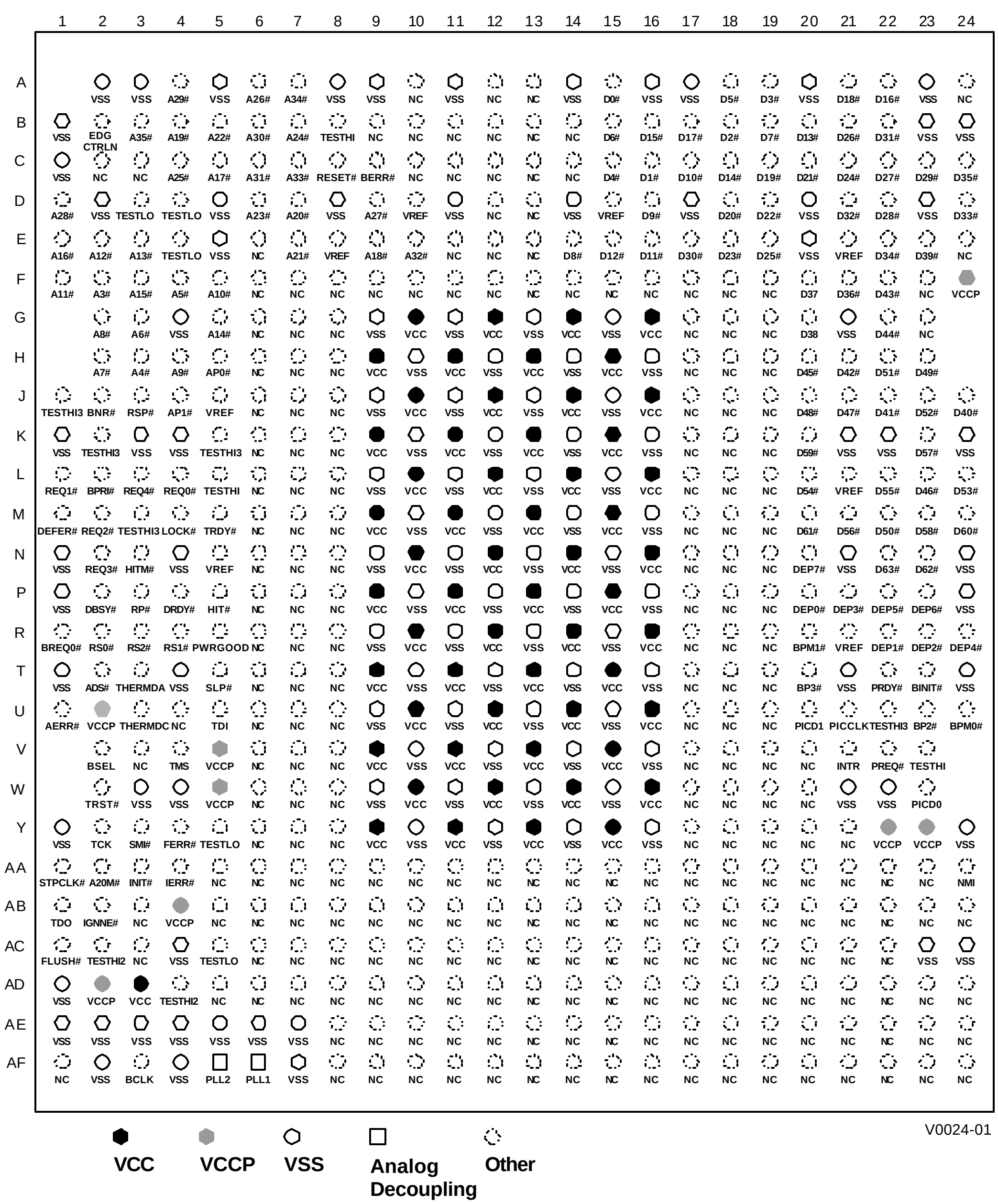


Figure 5.5 Pin/Ball Map - Top View

Table 5.3 Signal Listing in Order by Pin/Ball Number

Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name
A2	VSS	B8	TESTHI	C14	NC	D20	VSS
A3	VSS	B9	NC	C15	D4#	D21	D32#
A4	A29#	B10	NC	C16	D1#	D22	D28#
A5	VSS	B11	NC	C17	D10#	D23	VSS
A6	A26#	B12	NC	C18	D14#	D24	D33#
A7	A34#	B13	NC	C19	D19#	E1	A16#
A8	VSS	B14	NC	C20	D21#	E2	A12#
A9	VSS	B15	D6#	C21	D24#	E3	A13#
A10	NC	B16	D15#	C22	D27#	E4	TESTLO
A11	VSS	B17	D17#	C23	D29#	E5	VSS
A12	NC	B18	D2#	C24	D35#	E6	NC
A13	NC	B19	D7#	D1	A28#	E7	A21#
A14	VSS	B20	D13#	D2	VSS	E8	VREF
A15	D0#	B21	D26#	D3	TESTLO	E9	A18#
A16	VSS	B22	D31#	D4	TESTLO	E10	A32#
A17	VSS	B23	VSS	D5	VSS	E11	NC
A18	D5#	B24	VSS	D6	A23#	E12	NC
A19	D3#	C1	VSS	D7	A20#	E13	NC
A20	VSS	C2	NC	D8	VSS	E14	D8#
A21	D18#	C3	NC	D9	A27#	E15	D12#
A22	D16#	C4	A25#	D10	VREF	E16	D11#
A23	VSS	C5	A17#	D11	VSS	E17	D30#
A24	NC	C6	A31#	D12	NC	E18	D23#
B1	VSS	C7	A33#	D13	NC	E19	D25#
B2	EDGCTRLN	C8	RESET#	D14	VSS	E20	VSS
B3	A35#	C9	BERR#	D15	VREF	E21	VREF
B4	A19#	C10	NC	D16	D9#	E22	D34#
B5	A22#	C11	NC	D17	VSS	E23	D39#
B6	A30#	C12	NC	D18	D20#	E24	NC
B7	A24#	C13	NC	D19	D22#	F1	A11#

Table 5.3 Signal Listing in Order by Pin/Ball Number

Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name
F2	A3#	G8	NC	H15	VCC	J21	D47#
F3	A15#	G9	VSS	H16	VSS	J22	D41#
F4	A5#	G10	VCC	H17	NC	J23	D52#
F5	A10#	G11	VSS	H18	NC	J24	D40#
F6	NC	G12	VCC	H19	NC	K1	VSS
F7	NC	G13	VSS	H20	D45#	K2	TESTHI3
F8	NC	G14	VCC	H21	D42#	K3	VSS
F9	NC	G15	VSS	H22	D51#	K4	VSS
F10	NC	G16	VCC	H23	D49#	K5	TESTHI3
F11	NC	G17	NC	J1	TESTHI3	K6	NC
F12	NC	G18	NC	J2	BNR#	K7	NC
F13	NC	G19	NC	J3	RSP#	K8	NC
F14	NC	G20	D38#	J4	AP1#	K9	VCC
F15	NC	G21	VSS	J5	VREF	K10	VSS
F16	NC	G22	D44#	J6	NC	K11	VCC
F17	NC	G23	NC	J7	NC	K12	VSS
F18	NC	H2	A7#	J8	NC	K13	VCC
F19	NC	H3	A4#	J9	VSS	K14	VSS
F20	D37#	H4	A9#	J10	VCC	K15	VCC
F21	D36#	H5	AP0#	J11	VSS	K16	VSS
F22	D43#	H6	NC	J12	VCC	K17	NC
F23	NC	H7	NC	J13	VSS	K18	NC
F24	VCCP	H8	NC	J14	VCC	K19	NC
G2	A8#	H9	VCC	J15	VSS	K20	D59#
G3	A6#	H10	VSS	J16	VCC	K21	VSS
G4	VSS	H11	VCC	J17	NC	K22	VSS
G5	A14#	H12	VSS	J18	NC	K23	D57#
G6	NC	H13	VCC	J19	NC	K24	VSS

Table 5.3 Signal Listing in Order by Pin/Ball Number

Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name
G7	NC	H14	VSS	J20	D48#	L1	REQ1#
L2	BPRI#	M8	NC	N14	VCC	P20	DEP0#
L3	REQ4#	M9	VCC	N15	VSS	P21	DEP3#
L4	REQ0#	M10	VSS	N16	VCC	P22	DEP5#
L5	TESTHI	M11	VCC	N17	NC	P23	DEP6#
L6	NC	M12	VSS	N18	NC	P24	VSS
L7	NC	M13	VCC	N19	NC	R1	BREQ0#
L8	NC	M14	VSS	N20	DEP7#	R2	RS0#
L9	VSS	M15	VCC	N21	VSS	R3	RS2#
L10	VCC	M16	VSS	N22	D63#	R4	RS1#
L11	VSS	M17	NC	N23	D62#	R5	PWRGOOD
L12	VCC	M18	NC	N24	VSS	R6	NC
L13	VSS	M19	NC	P1	VSS	R7	NC
L14	VCC	M20	D61#	P2	DBSY#	R8	NC
L15	VSS	M21	D56#	P3	RP#	R9	VSS
L16	VCC	M22	D50#	P4	DRDY#	R10	VCC
L17	NC	M23	D58#	P5	HIT#	R11	VSS
L18	NC	M24	D60#	P6	NC	R12	VCC
L19	NC	N1	VSS	P7	NC	R13	VSS
L20	D54#	N2	REQ3#	P8	NC	R14	VCC
L21	VREF	N3	HITM#	P9	VCC	R15	VSS
L22	D55#	N4	VSS	P10	VSS	R16	VCC
L23	D46#	N5	VREF	P11	VCC	R17	NC
L24	D53#	N6	NC	P12	VSS	R18	NC
M1	DEFER#	N7	NC	P13	VCC	R19	NC
M2	REQ2#	N8	NC	P14	VSS	R20	BPM1#
M3	TESTHI3	N9	VSS	P15	VCC	R21	VREF
M4	LOCK#	N10	VCC	P16	VSS	R22	DEP1#
M5	TRDY#	N11	VSS	P17	NC	R23	DEP2#

Table 5.3 Signal Listing in Order by Pin/Ball Number

Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name
M6	NC	N12	VCC	P18	NC	R24	DEP4#
M7	NC	N13	VSS	P19	NC	T1	VSS
T2	ADS#	U8	NC	V15	VCC	W23	PICD0
T3	THERMDA	U9	VSS	V16	VSS	Y1	VSS
T4	VSS	U10	VCC	V17	NC	Y2	TCK
T5	SLP#	U11	VSS	V18	NC	Y3	SMI#
T6	NC	U12	VCC	V19	NC	Y4	FERR#
T7	NC	U13	VSS	V20	NC	Y5	TESTLO
T8	NC	U14	VCC	V21	INTR	Y6	NC
T9	VCC	U15	VSS	V22	PREQ#	Y7	NC
T10	VSS	U16	VCC	V23	TESTHI	Y8	NC
T11	VCC	U17	NC	W2	TRST#	Y9	VCC
T12	VSS	U18	NC	W3	VSS	Y10	VSS
T13	VCC	U19	NC	W4	VSS	Y11	VCC
T14	VSS	U20	PICD1	W5	VCCP	Y12	VSS
T15	VCC	U21	PICCLK	W6	NC	Y13	VCC
T16	VSS	U22	TESTHI3	W7	NC	Y14	VSS
T17	NC	U23	BP2#	W8	NC	Y15	VCC
T18	NC	U24	BPM0#	W9	VSS	Y16	VSS
T19	NC	V2	BSEL	W10	VCC	Y17	NC
T20	BP3#	V3	NC	W11	VSS	Y18	NC
T21	VSS	V4	TMS	W12	VCC	Y19	NC
T22	PRDY#	V5	VCCP	W13	VSS	Y20	NC
T23	BINIT#	V6	NC	W14	VCC	Y21	NC
T24	VSS	V7	NC	W15	VSS	Y22	VCCP
U1	AERR#	V8	NC	W16	VCC	Y23	VCCP
U2	VCCP	V9	VCC	W17	NC	Y24	VSS
U3	THERMDC	V10	VSS	W18	NC	AA1	STPCLK#
U4	NC	V11	VCC	W19	NC	AA2	A20M#

Table 5.3 Signal Listing in Order by Pin/Ball Number

Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name
U5	TDI	V12	VSS	W20	NC	AA3	INIT#
U6	NC	V13	VCC	W21	VSS	AA4	IERR#
U7	NC	V14	VSS	W22	VSS	AA5	NC
AA6	NC	AB12	NC	AC18	NC	AD24	NC
AA7	NC	AB13	NC	AC19	NC	AE1	VSS
AA8	NC	AB14	NC	AC20	NC	AE2	VSS
AA9	NC	AB15	NC	AC21	NC	AE3	VSS
AA10	NC	AB16	NC	AC22	NC	AE4	VSS
AA11	NC	AB17	NC	AC23	VSS	AE5	VSS
AA12	NC	AB18	NC	AC24	VSS	AE6	VSS
AA13	NC	AB19	NC	AD1	VSS	AE7	VSS
AA14	NC	AB20	NC	AD2	VCCP	AE8	NC
AA15	NC	AB21	NC	AD3	VCC	AE9	NC
AA16	NC	AB22	NC	AD4	TESTHI2	AE10	NC
AA17	NC	AB23	NC	AD5	NC	AE11	NC
AA18	NC	AB24	NC	AD6	NC	AE12	NC
AA19	NC	AC1	FLUSH#	AD7	NC	AE13	NC
AA20	NC	AC2	TESTHI2	AD8	NC	AE14	NC
AA21	NC	AC3	NC	AD9	NC	AE15	NC
AA22	NC	AC4	VSS	AD10	NC	AE16	NC
AA23	NC	AC5	TESTLO	AD11	NC	AE17	NC
AA24	NMI	AC6	NC	AD12	NC	AE18	NC
AB1	TDO	AC7	NC	AD13	NC	AE19	NC
AB2	IGNNE#	AC8	NC	AD14	NC	AE20	NC
AB3	NC	AC9	NC	AD15	NC	AE21	NC
AB4	VCCP	AC10	NC	AD16	NC	AE22	NC
AB5	NC	AC11	NC	AD17	NC	AE23	NC
AB6	NC	AC12	NC	AD18	NC	AE24	NC
AB7	NC	AC13	NC	AD19	NC	AF1	NC

Table 5.3 Signal Listing in Order by Pin/Ball Number

Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name	Pin/Ball No.	Signal Name
AB8	NC	AC14	NC	AD20	NC	AF2	VSS
AB9	NC	AC15	NC	AD21	NC	AF3	BCLK
AB10	NC	AC16	NC	AD22	NC	AF4	VSS
AB11	NC	AC17	NC	AD23	NC	AF5	PLL2
AF6	PLL1	AF11	NC	AF16	NC	AF21	NC
AF7	VSS	AF12	NC	AF17	NC	AF22	NC
AF8	NC	AF13	NC	AF18	NC	AF23	NC
AF9	NC	AF14	NC	AF19	NC	AF24	NC
AF10	NC	AF15	NC	AF20	NC		

Table 5.4 Signal Listing in Order by Signal Name

Pin/Ball No.	Signal Name	Signal Buffer Type	Pin/Ball No.	Signal Name	Signal Buffer Type
F2	A3#	Low Power GTL+ I/O	C7	A33#	Low Power GTL+ I/O
H3	A4#	Low Power GTL+ I/O	A7	A34#	Low Power GTL+ I/O
F4	A5#	Low Power GTL+ I/O	B3	A35#	Low Power GTL+ I/O
G3	A6#	Low Power GTL+ I/O	AA2	A20M#	2.5V CMOS Input
H2	A7#	Low Power GTL+ I/O	T2	ADS#	Low Power GTL+ I/O
G2	A8#	Low Power GTL+ I/O	U1	AERR#	Low Power GTL+ I/O
H4	A9#	Low Power GTL+ I/O	H5	AP0#	Low Power GTL+ I/O
F5	A10#	Low Power GTL+ I/O	J4	AP1#	Low Power GTL+ I/O
F1	A11#	Low Power GTL+ I/O	AF3	BCLK	Processor Clock Input
E2	A12#	Low Power GTL+ I/O	C9	BERR#	Low Power GTL+ I/O
E3	A13#	Low Power GTL+ I/O	T23	BINIT#	Low Power GTL+ I/O
G5	A14#	Low Power GTL+ I/O	J2	BNR#	Low Power GTL+ I/O
F3	A15#	Low Power GTL+ I/O	U23	BP2#	Low Power GTL+ I/O
E1	A16#	Low Power GTL+ I/O	T20	BP3#	Low Power GTL+ I/O
C5	A17#	Low Power GTL+ I/O	U24	BPM0#	Low Power GTL+ I/O
E9	A18#	Low Power GTL+ I/O	R20	BPM1#	Low Power GTL+ I/O
B4	A19#	Low Power GTL+ I/O	L2	BPRI#	Low Power GTL+ Input
D7	A20#	Low Power GTL+ I/O	R1	BREQ0#	Low Power GTL+ I/O
E7	A21#	Low Power GTL+ I/O	V2	BSEL	2.5V CMOS Input
B5	A22#	Low Power GTL+ I/O	A15	D0#	Low Power GTL+ I/O
D6	A23#	Low Power GTL+ I/O	C16	D1#	Low Power GTL+ I/O
B7	A24#	Low Power GTL+ I/O	B18	D2#	Low Power GTL+ I/O
C4	A25#	Low Power GTL+ I/O	A19	D3#	Low Power GTL+ I/O
A6	A26#	Low Power GTL+ I/O	C15	D4#	Low Power GTL+ I/O
D9	A27#	Low Power GTL+ I/O	A18	D5#	Low Power GTL+ I/O
D1	A28#	Low Power GTL+ I/O	B15	D6#	Low Power GTL+ I/O
A4	A29#	Low Power GTL+ I/O	B19	D7#	Low Power GTL+ I/O
B6	A30#	Low Power GTL+ I/O	E14	D8#	Low Power GTL+ I/O
C6	A31#	Low Power GTL+ I/O	D16	D9#	Low Power GTL+ I/O
E10	A32#	Low Power GTL+ I/O	C17	D10#	Low Power GTL+ I/O

Table 5.4 Signal Listing in Order by Signal Name

Pin/Ball No.	Signal Name	Signal Buffer Type	Pin/Ball No.	Signal Name	Signal Buffer Type
E16	D11#	Low Power GTL+ I/O	J22	D41#	Low Power GTL+ I/O
E15	D12#	Low Power GTL+ I/O	H21	D42#	Low Power GTL+ I/O
B20	D13#	Low Power GTL+ I/O	F22	D43#	Low Power GTL+ I/O
C18	D14#	Low Power GTL+ I/O	G22	D44#	Low Power GTL+ I/O
B16	D15#	Low Power GTL+ I/O	H20	D45#	Low Power GTL+ I/O
A22	D16#	Low Power GTL+ I/O	L23	D46#	Low Power GTL+ I/O
B17	D17#	Low Power GTL+ I/O	J21	D47#	Low Power GTL+ I/O
A21	D18#	Low Power GTL+ I/O	J20	D48#	Low Power GTL+ I/O
C19	D19#	Low Power GTL+ I/O	H23	D49#	Low Power GTL+ I/O
D18	D20#	Low Power GTL+ I/O	M22	D50#	Low Power GTL+ I/O
C20	D21#	Low Power GTL+ I/O	H22	D51#	Low Power GTL+ I/O
D19	D22#	Low Power GTL+ I/O	J23	D52#	Low Power GTL+ I/O
E18	D23#	Low Power GTL+ I/O	L24	D53#	Low Power GTL+ I/O
C21	D24#	Low Power GTL+ I/O	L20	D54#	Low Power GTL+ I/O
E19	D25#	Low Power GTL+ I/O	L22	D55#	Low Power GTL+ I/O
B21	D26#	Low Power GTL+ I/O	M21	D56#	Low Power GTL+ I/O
C22	D27#	Low Power GTL+ I/O	K23	D57#	Low Power GTL+ I/O
D22	D28#	Low Power GTL+ I/O	M23	D58#	Low Power GTL+ I/O
C23	D29#	Low Power GTL+ I/O	K20	D59#	Low Power GTL+ I/O
E17	D30#	Low Power GTL+ I/O	M24	D60#	Low Power GTL+ I/O
B22	D31#	Low Power GTL+ I/O	M20	D61#	Low Power GTL+ I/O
D21	D32#	Low Power GTL+ I/O	N23	D62#	Low Power GTL+ I/O
D24	D33#	Low Power GTL+ I/O	N22	D63#	Low Power GTL+ I/O
E22	D34#	Low Power GTL+ I/O	P2	DBSY#	Low Power GTL+ I/O
C24	D35#	Low Power GTL+ I/O	M1	DEFER#	Low Power GTL+ Input
F21	D36#	Low Power GTL+ I/O	P20	DEP0#	Low Power GTL+ I/O
F20	D37#	Low Power GTL+ I/O	R22	DEP1#	Low Power GTL+ I/O
G20	D38#	Low Power GTL+ I/O	R23	DEP2#	Low Power GTL+ I/O
E23	D39#	Low Power GTL+ I/O	P21	DEP3#	Low Power GTL+ I/O
J24	D40#	Low Power GTL+ I/O	R24	DEP4#	Low Power GTL+ I/O
P22	DEP5#	Low Power GTL+ I/O	R2	RS0#	Low Power GTL+ Input

Table 5.4 Signal Listing in Order by Signal Name

Pin/Ball No.	Signal Name	Signal Buffer Type	Pin/Ball No.	Signal Name	Signal Buffer Type
P23	DEP6#	Low Power GTL+ I/O	R4	RS1#	Low Power GTL+ Input
N20	DEP7#	Low Power GTL+ I/O	R3	RS2#	Low Power GTL+ Input
P4	DRDY#	Low Power GTL+ I/O	J3	RSP#	Low Power GTL+ Input
B2	EDGCTRLN	Low Power GTL+ Control	T5	SLP#	2.5V CMOS Input
Y4	FERR#	2.5V Open Drain Output	Y3	SMI#	2.5V CMOS Input
AC1	FLUSH#	2.5V CMOS Input	AA1	STPCLK#	2.5V CMOS Input
P5	HIT#	Low Power GTL+ I/O	Y2	TCK	JTAG Clock Input
N3	HITM#	Low Power GTL+ I/O	U5	TDI	JTAG Input
AA4	IERR#	2.5V Open Drain Output	AB1	TDO	JTAG Output
AB2	IGNNE#	2.5V CMOS Input	B8	TESTHI	GTL+ Test Input
AA3	INIT#	2.5V CMOS Input	L5	TESTHI	GTL+ Test Input
V21	INTR	2.5V CMOS Input	V23	TESTHI	GTL+ Test Input
M4	LOCK#	Low Power GTL+ I/O	AC2	TESTHI2	CMOS Test Input
AA24	NMI	2.5V CMOS Input	AD4	TESTHI2	CMOS Test Input
U21	PICCLK	APIC Clock Input	J1	TESTHI3	GTL+ Test Input
W23	PICD0	2.5V Open Drain I/O	K2	TESTHI3	GTL+ Test Input
U20	PICD1	2.5V Open Drain I/O	K5	TESTHI3	GTL+ Test Input
AF6	PLL1	PLL Analog Voltage	M3	TESTHI3	GTL+ Test Input
AF5	PLL2	PLL Analog Voltage	U22	TESTHI3	GTL+ Test Input
T22	PRDY#	Low Power GTL+ Output	D3	TESTLO	Test Input
V22	PREQ#	2.5V CMOS Input	D4	TESTLO	Test Input
R5	PWRGOOD	2.5V CMOS Input	E4	TESTLO	Test Input
L4	REQ0#	Low Power GTL+ I/O	Y5	TESTLO	Test Input
L1	REQ1#	Low Power GTL+ I/O	AC5	TESTLO	Test Input
M2	REQ2#	Low Power GTL+ I/O	T3	THERMDA	Thermal Diode Anode
N2	REQ3#	Low Power GTL+ I/O	U3	THERMDC	Thermal Diode Cathode
L3	REQ4#	Low Power GTL+ I/O	V4	TMS	JTAG Input
C8	RESET#	Low Power GTL+ Input	M5	TRDY#	Low Power GTL+ Input
P3	RP#	Low Power GTL+ I/O	W2	TRST#	JTAG Input
D10	VREF	GTL+ Reference Voltage	J5	VREF	GTL+ Reference Voltage
D15	VREF	GTL+ Reference Voltage	L21	VREF	GTL+ Reference Voltage

Table 5.4 Signal Listing in Order by Signal Name

Pin/Ball No.	Signal Name	Signal Buffer Type	Pin/Ball No.	Signal Name	Signal Buffer Type
E8	VREF	GTL+ Reference Voltage	N5	VREF	GTL+ Reference Voltage
E21	VREF	GTL+ Reference Voltage	R21	VREF	GTL+ Reference Voltage

Table 5.5 Voltage and No-Connect Pin/Ball Locations

Signal Name	Ball Numbers
NC	A10, A12, A13, A24, B9, B10, B11, B12, B13, B14, C2, C3, C10, C11, C12, C13, C14, D12, D13, E6, E11, E12, E13, E24, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F23, G6, G7, G8, G17, G18, G19, G23, H6, H7, H8, H17, H18, H19, J6, J7, J8, J17, J18, J19, K6, K7, K8, K17, K18, K19, L6, L7, L8, L17, L18, L19, M6, M7, M8, M17, M18, M19, N6, N7, N8, N17, N18, N19, P6, P7, P8, P17, P18, P19, R6, R7, R8, R17, R18, R19, T6, T7, T8, T17, T18, T19, U4, U6, U7, U8, U17, U18, U19, V3, V6, V7, V8, V17, V18, V19, V20, W6, W7, W8, W17, W18, W19, W20, Y6, Y7, Y8, Y17, Y18, Y19, Y20, Y21, AA5, AA6, AA7, AA8, AA9, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AA23, AB3, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AC3, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AD24, AE8, AE9, AE10, AE11, AE12, AE13, AE14, AE15, AE16, AE17, AE18, AE19, AE20, AE21, AE22, AE23, AE24, AF1, AF8, AF9, AF10, AF11, AF12, AF13, AF14, AF15, AF16, AF17, AF18, AF19, AF20, AF21, AF22, AF23, AF24
VCC	G10, G12, G14, G16, H9, H11, H13, H15, J10, J12, J14, J16, K9, K11, K13, K15, L10, L12, L14, L16, M9, M11, M13, M15, N10, N12, N14, N16, P9, P11, P13, P15, R10, R12, R14, R16, T9, T11, T13, T15, U10, U12, U14, U16, V9, V11, V13, V15, W10, W12, W14, W16, Y9, Y11, Y13, Y15, AD3
VCCP	F24, U2, V5, W5, Y22, Y23, AB4, AD2
VSS	A2, A3, A5, A8, A9, A11, A14, A16, A17, A20, A23, B1, B23, B24, C1, D2, D5, D8, D11, D14, D17, D20, D23, E5, E20, G4, G9, G11, G13, G15, G21, H10, H12, H14, H16, J9, J11, J13, J15, K1, K3, K4, K10, K12, K14, K16, K21, K22, K24, L9, L11, L13, L15, M10, M12, M14, M16, N1, N4, N9, N11, N13, N15, N21, N24, P1, P10, P12, P14, P16, P24, R9, R11, R13, R15, T1, T4, T10, T12, T14, T16, T21, T24, U9, U11, U13, U15, V10, V12, V14, V16, W3, W4, W9, W11, W13, W15, W21, W22, Y1, Y10, Y12, Y14, Y16, Y24, AC4, AC23, AC24, AD1, AE1, AE2, AE3, AE4, AE5, AE6, AE7, AF2, AF4, AF7

6. THERMAL SPECIFICATIONS

In order to achieve proper cooling of the processor, a thermal solution (for example a heat spreader, heat pipe, or other heat transfer system) must make firm contact to the exposed processor die.

The processor die must be clean before the thermal solution is attached or the processor may be damaged.

Table 6.1 Mobile Intel Celeron® Processor Power Specifications

Symbol	Parameter	Min	Typ[1]	Max	Unit	Notes
TDP	Thermal Design Power at 466 MHz		—	20.7	W	At 100°C [2,3]
	at 433 MHz		—	19.4	W	
	at 400 MHz		—	13.8	W	
	at 366 MHz		—	13.1	W	
	at 333 MHz		—	11.8	W	
	at 300 MHz		—	11.1	W	
	at 266 MHz		—	9.8	W	
	at 266 MHz at Low Voltage		—	7.9	W	
P_{SGNT}	Stop Grant and Auto Halt power at 400 MHz and Below at 433 and 466 MHz			1.25 2.00	W W	At 50°C [3]
P_{QS}	Quick Start and Sleep power at 400 MHz and Below at 433 and 466 MHz			0.50 0.80	W W	At 50°C [3]
P_{DSLP}	Deep Sleep power at 400 MHz and Below at 433 and 466 MHz			0.15 0.25	W W	At 50°C [3]
T_{CASE}	Case Temperature	0		100	°C	

NOTES:

1. TDP_{TYP} is a recommendation based on the power dissipation of the processor while executing publicly available software under normal operating conditions at nominal voltages. Contact your Intel Field Sales Representative for further information.
2. TDP_{MAX} is a specification of the total power dissipation of the processor while executing a worst-case instruction mix under normal operating conditions at nominal voltages. It includes the power dissipated by all of the components within the processor. Specified by design/characterization.
3. Not 100% tested or guaranteed. The power specifications are composed of the current of the processor on the various voltage planes. These currents are measured and specified at high temperature in Section 3.5. The 50°C power specifications are determined by characterization of the processor currents at higher temperatures.

During all operating environments, the processor case temperature, T_{CASE}, must be within the specified range of 0°C to 100°C. An A/D converter attached to the thermal diode can be used to measure the processor core temperature to ensure compliance with this specification. The designer is responsible for ensuring the thermal diode and A/D converter accurately tracks the processor temperature. The designer should verify this by correlating "sensor" output temperature with a thermocouple placed directly on the die surface. Refer to section 6.2 for more details.

6.1 Thermal Diode

The mobile Intel Celeron processor has an on-die diode that can be used to monitor the die temperature. A thermal sensor located on the system electronics may use the diode to monitor the die temperature of the mobile Intel Celeron processor for thermal management purposes. Table 6.2 and Table 6.3 provide the diode interface and specifications.

Table 6.2 Thermal Diode Interface

Signal Name	Ball Number	Signal Description
THERMDA	T3	Thermal diode anode
THERMDC	U3	Thermal diode cathode

Table 6.3. Thermal Diode Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5		500	mA	Note 1
n	Diode Ideality Factor	1.0000	1.0065	1.0173		Notes 2, 3, 4

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
2. At 35°C with a forward bias of 630mV.
3. Not 100% tested. Specified by design/characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode I/V equation:

$$I = I_O \cdot \left(e^{\frac{qV_D}{nkT}} - 1 \right)$$

6.2 Case Temperature

To verify that the proper T_{CASE} (case temperature) is maintained for the mobile Intel Celeron processor, it should be measured at the center of the die on the package top surface. To minimize any measurement errors, the following techniques are recommended:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the die on the top package surface using highly thermally conductive cements. Intel's laboratory testing was done using Omega Bond (part number: OB100). Thermal grease provides equivalent temperature measurement results when used correctly but is not as mechanically resilient as cement.
- The thermocouple should be attached at a 90° angle as shown in Figure 6.1. A horizontal thermocouple mount is acceptable.

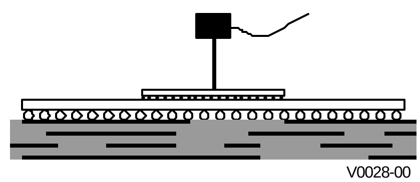


Figure 6.1 Technique for Measuring Case Temperature

7. PROCESSOR INITIALIZATION AND CONFIGURATION

7.1 Description

The mobile Intel Celeron processor has some configuration options that are determined by hardware and some that are determined by software. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET#. Most of the configuration options for the mobile Intel Celeron processor are identical to those of the Pentium II processor. The *Pentium® II Processor Developer's Manual* (order number 243502) describes these configuration options. New configuration options for the mobile Intel Celeron processor are described in the remainder of this section.

7.1.1 Quick Start Enable

The processor normally enters the Stop Grant state when the STPCLK# signal is asserted, but it will enter the Quick Start state instead if A15# is sampled active on the RESET# signal's active-to-inactive transition. The Quick Start state supports snoops from the bus priority device like the Stop Grant state, but it does not support symmetric master snoops, nor is the latching of interrupts supported. A '1' in bit position 5 of the Power-On Configuration register indicates that the Quick Start state has been enabled.

7.1.2 System Bus Frequency

The current generation mobile Intel Celeron processor will only function with a system bus frequency of 66 MHz, but future generations may operate at 100 MHz. Bit position 19 of the Power-On Configuration register indicates at which speed a processor will run. A '0' in bit 19 indicates a 66-MHz bus frequency and a '1' indicates a 100-MHz bus frequency.

7.1.3 APIC Disable

The APIC has been removed as a feature of the mobile Intel Celeron processor. The PICCLK and PICD[1:0] signals must be tied to V_{SS} with a 1KΩ resistor to disable the APIC. Driving PICD0 low at reset has the effect of clearing the APIC Global Enable bit in the APIC Base MSR. This bit is normally set when the processor is reset, but when it is cleared the APIC is completely disabled until the next reset.

7.2 Clock Frequencies and Ratios

The mobile Intel Celeron processor uses a clock design in which the bus clock is multiplied by a ratio to produce the processor's internal (or "core") clock. The ratio used is programmed into the processor during Reset. Section 3.3 describes how this is done. The bus ratio programmed into the processor is visible in bit positions 22 to 25 of the Power-On Configuration register. Table 3.4 shows the 4-bit codes in the Power-On Configuration register and their corresponding bus ratios.

8. PROCESSOR INTERFACE

8.1 Alphabetical Signal Reference

A[35:3]# (I/O - Low Power GTL+)

The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal.

On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 7 of this document and the *Pentium® II Processor Developer's Manual* for details.

A20M# (I - 2.5V tolerant)

If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.

During active RESET#, the processor begins sampling the A20M#, IGNNE#, INTR, and NMI values to determine the ratio of core-clock frequency to bus-clock frequency (see Table 3.4). On the active-to-inactive transition of RESET#, the processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.

ADS# (I/O - Low Power GTL+)

The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate balls on both agents on the system bus.

AERR# (I/O - Low Power GTL+)

The AERR# (Address Parity Error) signal is observed and driven by both system bus agents and if used, must be connected to the appropriate balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction.

If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.

The AERR# processor bus pin is removed as a processor feature for mobile Intel Celeron processor at 400 MHz and above. The pin must still be terminated to Vcc through a 120Ω pull-up resistor. But the processor must not be configured to drive or observe the pin.

AP[1:0]# (I/O - Low Power GTL+)

The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate balls on both agents on the system bus.

BCLK (I - 2.5V tolerant)

The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

BERR# (I/O - Low Power GTL+)

The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate balls of both agents, if used. However, mobile Intel Celeron processors do not observe assertions of the BERR# signal.

BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:

- Enabled or disabled
- Asserted optionally for internal errors along with IERR#
- Asserted optionally by the request initiator of a bus transaction after it observes an error
- Asserted by any bus agent when it observes an error in a bus transaction

BINIT# (I/O - Low Power GTL+)

The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

If BINIT# is enabled during power-on configuration and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.

BNR# (I/O - Low Power GTL+)

The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal which must be connected to the appropriate balls of both agents on the system bus. In order to avoid wire-OR errors associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.

BP[3:2]# (I/O - Low Power GTL+)

The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.

BPM[1:0]# (I/O - Low Power GTL+)

The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

BPRI# (I - Low Power GTL+)

The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the

processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.

BREQ0# (I/O - Low Power GTL+)

The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal.

During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#.

BSEL (I - 2.5V Tolerant)

The BSEL (System Bus Speed Select) signal is used to configure the processor for the system bus frequency. A ‘1’ on this signal configures the processor for 100-MHz operation and a ‘0’ configures it for 66-MHz operation. This signal must be connected to V_{SS}.

D[63:0]# (I/O - Low Power GTL+)

The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

DBSY# (I/O - Low Power GTL+)

The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate balls on both agents on the system bus.

DEFER# (I - Low Power GTL+)

The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate balls on both agents on the system bus.

DEP[7:0]# (I/O - Low Power GTL+)

The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]# and must be connected to the appropriate balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.

DRDY# (I/O - Low Power GTL+)

The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate balls on both agents on the system bus.

EDGCTRLN (Analog)

This signal is used to configure the edge rate of the Low Power GTL+ output buffers. Connect the EDGCTRLN (Edge Rate Control N-FET) signal to V_{CC} with a 51-Ω, 1-% resistor.

FERR# (O - 2.5V Tolerant Open-drain)

The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel387 coprocessor and is included for compatibility with systems using DOS-type floating-point error reporting.

FLUSH# (I - 2.5V Tolerant)

When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted.

On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power- on configuration.

HIT# (I/O - Low Power GTL+), HITM# (I/O - Low Power GTL+)

The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

IERR# (O - 2.5V Tolerant Open-drain)

The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.

IGNNE# (I - 2.5V Tolerant)

The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.

During active RESET#, the processor begins sampling the A20M#, IGNNE#, INTR, and NMI values to determine the ratio of core-clock frequency to bus-clock frequency (see Table 3.4). On the active-to-inactive transition of RESET#, the processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.

INIT# (I - 2.5V Tolerant)

The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input.

If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

INTR (I - 2.5V Tolerant)

The INTR (Interrupt) signal indicates that an external interrupt has been generated. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition. INTR must be deasserted for a minimum of two clocks to guarantee its inactive recognition.

During active RESET#, the processor begins sampling the A20M#, IGNNE#, INTR, and NMI values to determine the ratio of core-clock frequency to bus-clock frequency (see Table 3.4). On the active-to-inactive transition of RESET#, the

processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.

LOCK# (I/O - Low Power GTL+)

The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction.

When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.

NMI (I - 2.5V Tolerant)

The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending.

NMI is rising-edge sensitive. Active and inactive pulse widths must be a minimum of two clocks.

During active RESET#, the processor begins sampling the A20M#, IGNNE#, INTR, and NMI values to determine the ratio of core-clock frequency to bus-clock frequency (see Table 3.4). On the active-to-inactive transition of RESET#, the processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.

PICCLK (I - 2.5V Tolerant)

The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic and I/O APIC components on the APIC bus.

PICD[1:0] (I/O - 2.5V Tolerant Open-drain)

The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.

PRDY# (O - Low Power GTL+)

The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.

PREQ# (I - 2.5V Tolerant)

The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.

PWRGOOD (I - 2.5V Tolerant)

PWRGOOD (Power Good) is a 2.5V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (V_{CC}, V_{CCP}, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure 8.1 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must

also meet the minimum pulse width specified in Table 3.14 (Section 3.5), and be followed by a 1 ms RESET# pulse.

The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

REQ[4:0]# (I/O - Low Power GTL+)

The REQ[4:0]# (Request Command) signals must be connected to the appropriate balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.

RESET# (I - Low Power GTL+)

Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines.

For a power-on type reset, RESET# must stay active for at least 1 msec after V_{CC} and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks.

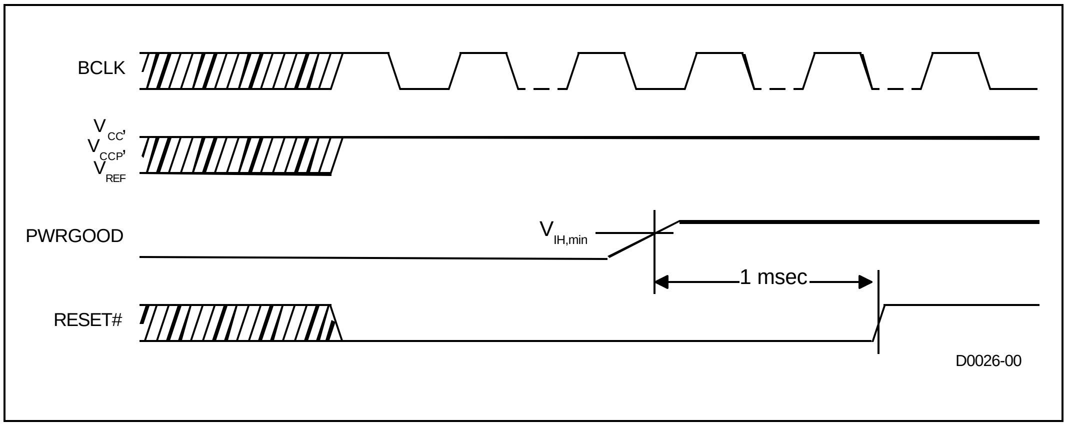


Figure 8.1 PWRGOOD Relationship at Power-On

A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 7 and in the *Pentium® II Processor Developer's Manual*.

Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate balls on both agents on the system bus.

RP# (I/O - Low Power GTL+)

The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

RS[2:0]# (I - Low Power GTL+)

The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for

completion of the current transaction) and must be connected to the appropriate balls on both agents on the system bus.

RSP# (I - Low Power GTL+)

The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.

SLP# (I - 2.5V Tolerant)

The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK#, and RESET# signals while in the Sleep state.

If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.

SMI# (I - 2.5V Tolerant)

The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.

STPCLK# (I - 2.5V Tolerant)

The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction, and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock.

TCK (I - 2.5V Tolerant)

The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

TDI (I - 2.5V Tolerant)

The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.

TDO (O - 2.5V Tolerant Open-drain)

The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.

THERMDA, THERMDC (Analog)

The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.

TMS (I - 2.5V Tolerant)

The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.

TRDY# (I - Low Power GTL+)

The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit writeback data transfer. TRDY# must be connected to the appropriate balls on both agents on the system bus.

TRST# (I - 2.5V Tolerant)

The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Mobile Intel Celeron processors do not self- reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

8.2 Signal Summaries

Table 8.1 through Table 8.4 list the attributes of the processor input, output, and I/O signals.

Table 8.1 Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS	Always
BCLK	High	—	System Bus	Always
BPRI#	Low	BCLK	System Bus	Always
DEFER#	Low	BCLK	System Bus	Always
FLUSH#	Low	Asynch	CMOS	Always
IGNNE#	Low	Asynch	CMOS	Always
INIT#	Low	Asynch	System Bus	Always
INTR	High	Asynch	CMOS	APIC disabled mode
NMI	High	Asynch	CMOS	APIC disabled mode
PICCLK	High	—	APIC	Always
PREQ#	Low	Asynch	Implementation	Always
PWRGOOD	High	Asynch	Implementation	Always
RESET#	Low	BCLK	System Bus	Always
RS[2:0]#	Low	BCLK	System Bus	Always
RSP#	Low	BCLK	System Bus	Always
BSEL	High	Asynch	Implementation	Always
SLP#	Low	Asynch	Implementation	Stop Grant state

Table 8.1 Input Signals

Name	Active Level	Clock	Signal Group	Qualified
SMI#	Low	Asynch	CMOS	Always
STPCLK#	Low	Asynch	Implementation	Always
TCK	High	—	JTAG	
TDI		TCK	JTAG	
TMS		TCK	JTAG	
TRDY#	Low	BCLK	System Bus	Response phase
TRST#	Low	Asynch	JTAG	

Table 8.2 Output Signals

Name	Active Level	Clock	Signal Group
FERR#	Low	Asynch	Open-Drain
IERR#	Low	Asynch	Open-Drain
PRDY#	Low	BCLK	Implementation
TDO	High	TCK	JTAG

Table 8.3 Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:3]#	Low	BCLK	System Bus	ADS#, ADS#+1
ADS#	Low	BCLK	System Bus	Always
AP[1:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
BREQ0#	Low	BCLK	System Bus	Always
BP[3:2]#	Low	BCLK	System Bus	Always
BPM[1:0]#	Low	BCLK	System Bus	Always
D[63:0]#	Low	BCLK	System Bus	DRDY#

Table 8.3 Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
DBSY#	Low	BCLK	System Bus	Always
DEP[7:0]#	Low	BCLK	System Bus	DRDY#
DRDY#	Low	BCLK	System Bus	Always
LOCK#	Low	BCLK	System Bus	Always
REQ[4:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
RP#	Low	BCLK	System Bus	ADS#, ADS#+1

Table 8.4 Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	System Bus	ADS#+3
BERR#	Low	BCLK	System Bus	Always
BINIT#	Low	BCLK	System Bus	Always
BNR#	Low	BCLK	System Bus	Always
HIT#	Low	BCLK	System Bus	Always
HITM#	Low	BCLK	System Bus	Always
PICD[1:0]	High	PICCLK	APIC	Always